ADM6996F

6 Port 10/100 Mbit/s Single Chip Ethernet Switch Controller

ADM6996F, Version AA

Communication CPE

Never stop thinking.

The information in this document is subject to change without notice.

Edition 2005-07-04

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
81669 München, Germany

Attention please!

The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

ADM6996F, 6 Port 10/100 Mbit/s Single Chip Ethernet Switch Controller

Revision History: 2005-07-04, Rev. 1.17

Previous Version: 1.05

Page/Date	Subjects (major changes since last revision)
	Rev. 1.15: Changed to Infineon format
	Rev. 1.16: Improvements to contents. Additional information on Pin Descriptions, PHY Register descriptions and MAC MII Connections added. No major changes.
2005-07-04	Rev. 1.17: Changes to the new Infineon format

Trademarks

Table of Contents

Table of Contents

List of Figures

List of Tables

1 Product Overview

1.1 ADM6996F Overview

The ADM6996F is a high performance, low cost, highly integrated (Controller, PHY and Memory) four-port 10/100 Mbit/s TX/FX plus two 10/100 MAC port Ethernet switch controller with all ports supporting 10/100 Mbit/s Full/Half duplex operation. The ADM6996F is intended for applications such as stand alone bridges for the low cost SOHO markets such as 5-port switches and router applications. The 2nd MAC can be configured as a PCS type MII with an integrated 10/100 PHY.

The ADM6996F provides functions such as: 802.1p(Q.O.S.), Port-based/Tag-based VLAN, Port MAC address locking, management, port status, TP auto-MDIX, 25M crystal & extra MII port functions to meet customer requests on switch demand.

The ADM6996F also supports back pressure in Half-Duplex mode and the 802.3x Flow Control Pause packet in Full-Duplex mode to prevent packet loss when buffers are full. When Back Pressure is enabled, and there is no receive buffer available for the incoming packet, the ADM6996F will issue a JAM pattern on the receiving port in Half Duplex mode and issue the 802.3x Pause packet back to the receiving end in Full Duplex mode.

The built-in SRAM used for the packet buffer is divided into 256 bytes per block to achieve the optimized memory utilization through complicated link lists on packets with various lengths.

The ADM6996F also supports priority features using Port-Based, VLAN and IP TOS field checking. Users can easily set different priority modes in individual ports, through a small low-cost micro controller when initializing or configure on-the-fly. Each output port supports four queues in the way of fixed 8:4:2:1 fairness queuing to fit the bandwidth demand on various types of packets such as Voice, Video and Data. Tag Insert/Remove, and up to 16 groups of VLAN are also supported.

An intelligent address recognition algorithm allows ADM6996F to recognize up to 2K different MAC addresses and enables filtering and forwarding at full wire speed.

Port MAC address Locking function is also supported by ADM6996F to use on building Internet access to prevent multiple users sharing one port.

1.2 Features

- Supports five 10M/100M auto-detect Half/Full duplex switch ports with TX/FX interfaces and one MII/GPSI port.
- Supports 2K MAC addresses table with 1-ways associative hash algorithm.
- Supports four queue for QoS
- Supports priority features by Port-Based, 802.1p, IP TOS of packets.
- Supports Store & Forward architecture and performs forwarding and filtering at non-blocking full wire speed.
- Supports buffer allocation with 256 bytes per block
- Supports Aging function Enable/Disable.
- Supports 802.3x Flow Control pause packet for Full Duplex in case buffer is full.
- Supports Back Pressure function for Half Duplex operation in case buffer is full.
- Supports packet length up to 1518/1522 (Default) bytes in maximum.
- Broadcast Storm Suppression.
- Supports Tag-based VLAN. Up to 16 VLAN groups are implemented by the last four bits of VLAN ID.
- 2bit MAC clone to support multiple WAN application
- Supports TP interface Auto MDIX function for auto TX/RX swap by strapping-pin.
- Easy Management 32bits smart counter for per port RX/TX byte/packet count, 16-bit smart counter for per port ERROR count and Collision count .
- Supports PHY status output for management system.

- 25M Crystal only for the whole system.
- 128 QFP package with 0.18um technology. 1.8 V/3.3 V power supply.
- 1.4 W low power consumption.

1.3 Applications

ADM6996F:

- SOHO 5-port switch
- 5-port switch + Router with 2 MII CPU interface.

1.4 Block Diagram

Figure 1 below shows a simple block diagram of the ADM6996F internal blocks.

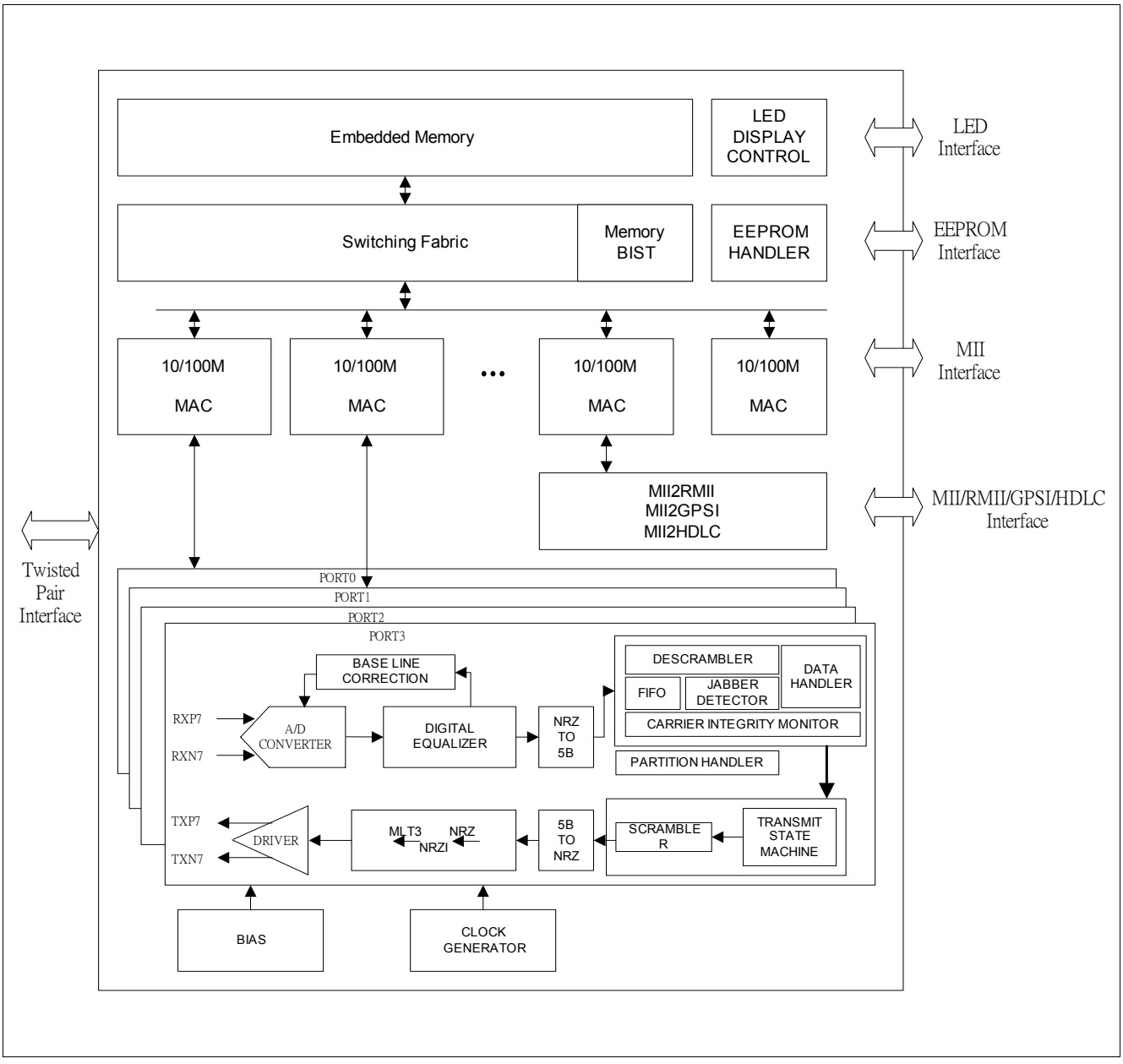


Figure 1 ADM6996F Block Diagram

2 Interface Description

This chapter describes the interface descriptions for the ADM6996F

- Pin Diagram
- Abbreviations
- Pin Description by Function

2.1 Pin Diagram

Figure 2 shows the pin diagram for the ADM6996F.

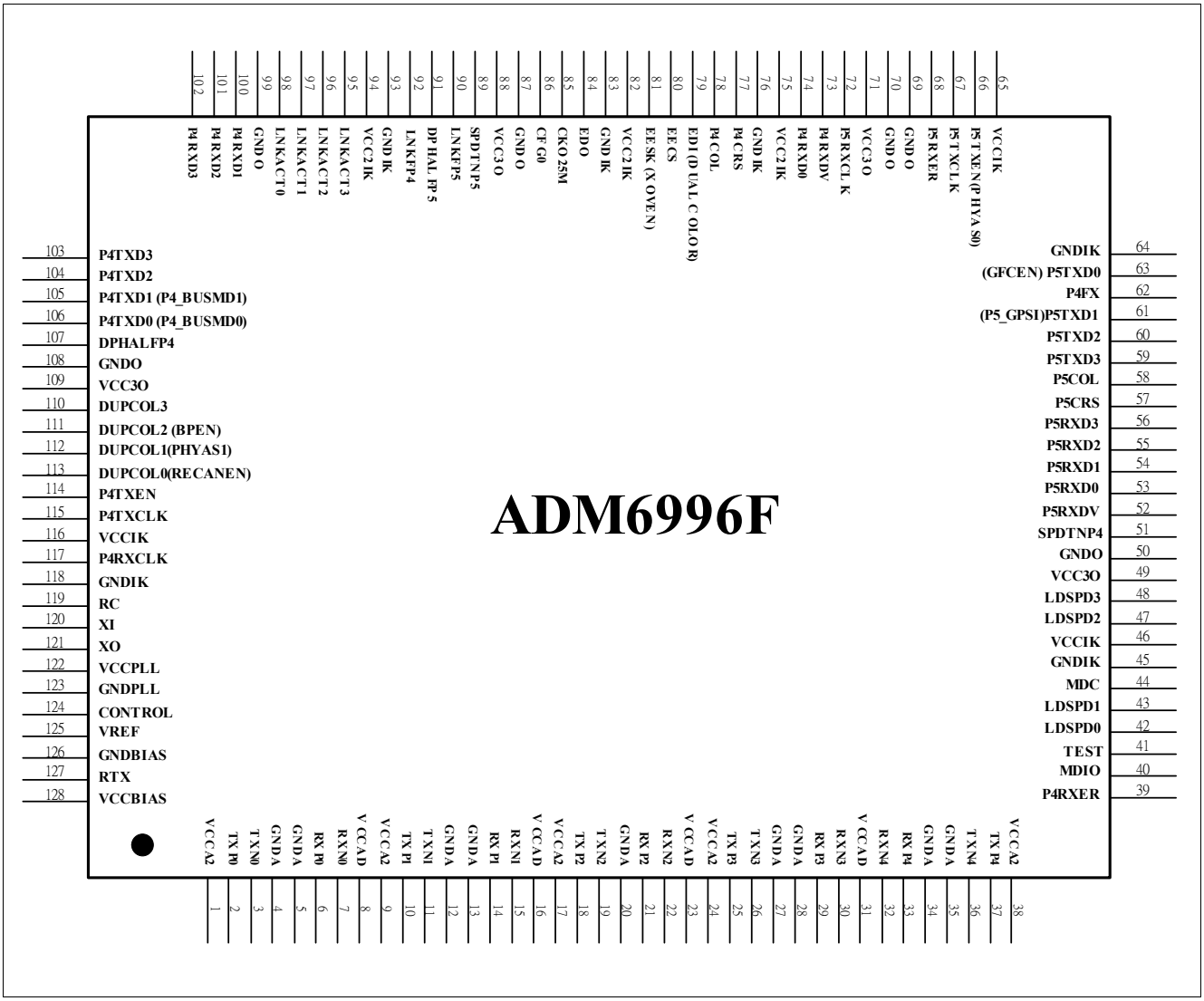


Figure 2 4 TP/FX PORT + 2 MII PORT 128 Pin Diagram

2.2 Abbreviations

Standard abbreviations for I/O tables:

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU	Pull up, 10 kΩ
PD	Pull down, 10 kΩ
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.3 Pin Description by Function

ADM6996F pins are categorized into one of the following groups:

- Network Media Connection
- Port 4 MII Interface
- Port 5 MII Interface
- LED Interface
- EEPROM Interface
- Power/Ground, 48 pins
- Miscellaneous

*Note: **Table 1** can be used for reference.*

Table 3 IO Signals

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Network Media Connection				
33	RXP_4	AI/O	ANA	**Receive Pair** Differential data is received on this pin.
29	RXP_3			
21	RXP_2			
14	RXP_1			
6	RXP_0			
32	RXN_4	AI/O	ANA	
30	RXN_3			
22	RXN_2			
15	RXN_1			
7	RXN_0			
37	TXP_4	AI/O	ANA	**Transmit Pair** Differential data is transmitted on this pin.
25	TXP_3			
18	TXP_2			
10	TXP_1			
2	TXP_0			
36	TXN_4	AI/O	ANA	
26	TXN_3			
19	TXN_2			
11	TXN_1			
3	TXN_0			
Port 4 MII Interface				
74	MMII_P4RXD0	I	PD, LVTTL	**Port 4 Receive Data Bit 0 in MAC MII Mode** In MAC MII mode, the bit is the LSB of MII receive data, synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXD0	O	8 mA, PD, LVTTL	**Port 4 Receive Data Bit 0 in PCS MII Mode** When port 4 is operating in PCS MII mode, the bit is the LSB of MII receive data output and synchronous to the rising edge of PMII_P4RXCLK.
102	MMII_P4RXD3	I	PD, LVTTL	**Port 4 Receive Data Bit 3 in MAC MII Mode** In MAC MII mode, this bit is bit[3] of MII receive data, and synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXD3	O	8 mA, PD, LVTTL	**Port 4 Receive Data Bit 3 in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is bit[3] of MII receive data output and synchronous to the rising edge of PMII_P4RXCLK.

Table 3 IO Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
101	MMII_P4RXD2	I	PD, LVTTL	**Port 4 Receive Data Bit 2 in MAC MII Mode** In MAC MII mode, this pin is bit[2] of MII receive data, and synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXD2	O	8 mA, PD, LVTTL	**Port 4 Receive Data Bit 2 in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is bit[2] of MII receive data output and synchronous to the rising edge of PMII_P4RXCLK.
100	MMII_P4RXD1	I	PD, LVTTL	**Port 4 Receive Data Bit 1 in MAC MII Mode** In MAC MII mode, this pin is bit[1] of MII receive data, and synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXD1	O	8 mA, PD, LVTTL	**Port 4 Receive Data Bit 1 in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is bit[1] of MII receive data output and synchronous to the rising edge of PMII_P4RXCLK.
73	MMII_P4RXDV	I	PD, LVTTL	**Port 4 Receive Data Valid in MAC MII Mode** Active high to indicate that the data on MMII_P4RXD[3:0] is valid. Synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXDV	O	8 mA, PD, LVTTL	**Port 4 Receive Data Valid in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is an active high output signal to indicate PMII_P4RXD[3:0] is valid. Synchronous to the rising edge of PMII_P4RXCLK.
39	MII_P4RXER	I	PD, LVTTL	**Port 4 Receive Error in MAC MII Mode** Active high to indicate that there is symbol error on the MII_P4RXD [3:0]. Only valid in 100M operation.
77	MMII_P4CRS	I	PD, LVTTL	**Port 4 Carrier Sense in MAC MII Mode** In full duplex mode, MMII_P4CRS reflects the receive carrier sense situation on medium only; In Half Duplex, CRS will be high both in receive and transmit condition.
	PMII_P4CRS	O	8 mA, PD, LVTTL	**Port 4 Carrier Sense in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is used to output Carrier Sense status.
78	MMII_P4COL	I	PD, LVTTL	**Port 4 Collision input in MAC MII Mode** Active high to indicate that there is collision on the medium. Stay low in full duplex operation.
	PMII_P4COL	O	8 mA, PD, LVTTL	**Port 4 Collision output in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is used to output collision status.

Table 3 IO Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
106	P4_BUSMD0	I	PD, LVTTL	**Port 4 Bus Type Configuration 0** Value on this pin will be latched by ADM6996F at the rising edge of RESETL(**RC**) for Port 4 Configuration Bit 0. Combined with **CFG0** and **P4_BUSMD1**, ADM6996F provides 4 bus type for port 4. See **CFG0** pin description for more detail. *Note: Power On Setting*
	MMII_P4TXD0	O	8 mA, PD, LVTTL	**Port 4 Transmit Data Bit 0 in MAC MII Mode** The LSB bit of MAC MII Transmit data of port 4. Synchronous to the rising edge of MMII_P4TXCLK.
	PMII_P4TXD0	I	PD, LVTTL	**Port 4 Transmit Data Bit 0 in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is the LSB of MII transmit data input and synchronous to the rising edge of PMII_P4TXCLK.
105	P4_BUSMD1	I	PD, LVTTL	**Port 4 Bus Type Configuration 1** Value on this pin will be latched by ADM6996F at the rising edge of RESETL(**RC**) for Port 4 Configuration Bit 1. Combined with **CFG0** and **P4_BUSMD0**, ADM6996F provides 4 bus type for port 4. See **CFG0** for more detail. *Note: Power On Setting*
	MMII_P4TXD1	O	8 mA, PD, LVTTL	**Port 4 Transmit Data Bit 1 in MAC MII Mode** The bit[1] of MAC MII Transmit data of port 4. Synchronous to the rising edge of MMII_P4TXCLK.
	PMII_P4TXD1	I	PD, LVTTL	**Port 4 Transmit Data Bit 1 in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is bit[1] of MII transmit data input and synchronous to the rising edge of PMII_P4TXCLK.
103	MMII_P4TXD3	O	8 mA, PD, LVTTL	**Port 4 Transmit Data Bit 3 in MAC MII Mode** The bit[3] of MAC MII Transmit data of port 4. Synchronous to the rising edge of MMII_P4TXCLK.
	PMII_P4TXD3	I	PD, LVTTL	**Port 4 Transmit Data Bit 3 in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is bit[3] of MII transmit data input and synchronous to the rising edge of PMII_P4TXCLK.
104	MMII_P4TXD2	O	8 mA, PD, LVTTL	**Port 4 Transmit Data Bit 2 in MAC MII Mode** The bit [2] of MAC MII Transmit data of port 4. Synchronous to the rising edge of MMII_P4TXCLK.
	PMII_P4TXD2	I	PD, LVTTL	**Port 4 Transmit Data Bit 2 in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is bit[2] of MII transmit data input and synchronous to the rising edge of PMII_P4TXCLK.

Table 3 IO Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
114	MMII_P4TXEN	O	8 mA, PD, LVTTL	**Port 4 Transmit Enable in MAC MII Mode** Output by ADM6996F at the rising edge of MMII_P4TXCLK when ADM6996F is programmed to MAC Type MII.
	PMII_P4TXEN	I	PD, LVTTL	**Port 4 Transmit Enable in PCS MII Mode** It is the MII Transmit Enable input to ADM6996F when programmed to PCS Type MII.
117	MMII_P4RXCLK	I	PD, LVTTL	**Port 4 Receive Clock in MAC MII Mode** 25MHz Free Running clock in 100M Mode and 2.5MHz free running clock in 10M Mode. MMII_P4RXDV and MMII_P4RXD[3:0] should be synchronous to the rising edge of this clock
	PMII_P4RXCLK	O	8 mA, PD, LVTTL	**Port 4 Receive Clock in PCS MII Mode** 25MHz Free Running clock in 100M Mode and 2.5MHz free running clock in 10M Mode. PMII_P4RXDV and PMII_P4RXD[3:0] should be synchronous to the rising edge of this clock
115	MMII_P4TXCLK	I	PD, LVTTL	**Port 4 Transmit Clock in MAC MII Mode** 25MHz Free Running clock in 100M Mode and 2.5MHz free running clock in 10M Mode. MMII_P4TXEN and MMII_P4TXD[3:0] should be synchronous to the rising edge of this clock
	PMII_P4TXCLK	O	8 mA, PD, LVTTL	**Port 4 Transmit Clock in PCS MII Mode** 25MHz Free Running clock in 100M Mode and 2.5MHz free running clock in 10M Mode. PMII_P4TXEN and PMII_P4TXD[3:0] should be synchronous to the rising edge of this clock
62	P4FX	I	PD, LVTTL	**Port 4 Fiber Selection for PCS MII/PHY mode** During power on reset, value will be latched by ADM6996F at the rising edge of RESETL(**RC**) as port 4 Fiber select . 0_B , Twisted Pair Mode 1_B , Fiber Mode
Port 5 MII Interface				

Table 3 IO Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
63	GFCEN	I	PU, LVTTL	**Global Flow Control Enable** Value on this pin will be latched by ADM6996F at the rising edge of RESETL(**RC**) as Flow control enable. *Note: Power On Setting* 0_B , Flow Control Capability is depended upon the register setting in corresponding port's Basic Control Register 1_B , All ports flow control capability is enabled
	MII_P5TXD0	O	4 mA, PU, LVTTL	**Port 5 Transmit Data Bit 0 in MII Mode** The LSB bit of MII Transmit data of port 5. Synchronous to the rising edge of MII_P5TXCLK.
	GPSI_P5TXD	O	4 mA, PU, LVTTL	**Port 5 Transmit Data in GPSI Mode** When port 5 is operating in GPSI mode, this pin acts as GPSI Transmit Data. Synchronous to the rising edge of GPSI_P5TXCLK.
61	P5_GPSI	I	PD, LVTTL	**Port 5 Bus Mode GPSI Selection** Value on this pin will be latched by ADM6996F at the rising edge of RESETL(**RC**) as port 5 bus mode GPSI selection. P5_GPSI, Interface *Note: Power On Setting* 0_B , MII 1_B , GPSI
	MII_P5TXD1	O	4 mA, PD, LVTTL	**Port 5 Transmit Data Bit 1 in MII Mode** The Second bit of MII Transmit data of port 5. Synchronous to the rising edge of MII_P5TXCLK.
60	MII_P5TXD2	O	4 mA, PD, LVTTL	**Port 5 Transmit Data Bit 2 in MII Mode** The Third bit of MII Transmit data of port 5. Synchronous to the rising edge of MII_P5TXCLK.
59	MII_P5TXD3	O	4 mA, PD, LVTTL	**Port 5 Transmit Data Bit 3 in MII Mode** The MSB bit of MII Transmit data of port 5. Synchronous to the rising edge of MII_P5TXCLK.

Table 3 IO Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
66	PHYAS0	I	PD, LVTTL	**PHY Address MSB Bit 0** During power on reset, value will be latched by ADM6996F at the rising edge of RESETL(**RC**) as the master/slave mode select. In master mode, ADM6996F will drive out the EEPROM control signals. PHYAS[1:0] = 00_B and PHY address start from 01000_B PHYAS[1:0], Interface *Note: Power On Setting* 00_B , Master (EEPROM 0x00h~0x3fh and SMI 00) 01_B , Slave (EEPROM 0x40h~0x7fh and SMI 01) 10_B , Slave (EEPROM 0x80h~0xbfh and SMI 10)l 11_B , Slave (EEPROM 0xc0h~0xffh and SMI 11)
	MII_P5TXEN	O	8 mA, PD, LVTTL	**Port 5 Transmit Enable TXEN in MII Mode** Active high to indicate that the data on MII_P5TXD[3:0] is valid. Synchronous to the rising edge of MII_P5TXCLK.
	GPSI_P5TXEN	O	8 mA, PD, LVTTL	**Port 5 Transmit Enable TXEN in GPSI Mode** Active high to indicate that the data on GPSI_P5TXD is valid. Synchronous to the rising edge of GPSI_P5TXCLK.
53	MII_P5RXD0	I	PD, LVTTL	**Port 5 Receive Data Bit 0 in MII Mode** In MII mode, the bit is the LSB of MII receive data, synchronous to the rising edge of MII_P5RXCLK.
	GPSI_P5RXD	I	PD, LVTTL	**Port 5 Receive Data in GPSI Mode** In GPSI Mode, this acts as Receive Data Input, synchronous to the rising edge of GPSI_P5RXCLK.
54	MII_P5RXD1	I	PD, LVTTL	**Port 5 Receive Data Bit 1 in MII Mode** In MII mode, the bit is the LSB of MII receive data, synchronous to the rising edge of MII_P5RXCLK.
55	MII_P5RXD2	I	PD, LVTTL	**Port 5 Receive Data Bit 2 in MII Mode** In MII mode, the bit is the bit[2] of MII receive data. Synchronous to the rising edge of MII_P5RXCLK.
56	MII_P5RXD3	I	PD, LVTTL	**Port 5 Receive Data Bit 3 in MII Mode** In MII mode, the bit is the bit[3] of MII receive data. Synchronous to the rising edge of MII_P5RXCLK.
52	MII_P5RXDV	I	PD, LVTTL	**Port 5 Receive Data Valid in MII Mode** Active high to indicate that the data on MII_P5RXD[3:0] is valid. Synchronous to the rising edge of MII_P5RXCLK.
68	MII_P5RXER	I	PD, LVTTL	**Port 5 Receive Error in MII Mode** Active high to indicate that there is a symbol error on the MII_P5RXD [3:0]. Only valid in 100M operation.

Table 3 IO Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
57	MII_P5CRS	I	PD, LVTTL	**Port 5 Carrier Sense in MII Mode** In full duplex mode, MII_P5CRS reflects the receive carrier sense situation on medium only; In Half Duplex, MII_P5CRS will be high both in receive and transmit condition.
	GPSI_P5CRS	I	PD, LVTTL	**Port 5 Carrier Sense in GPSI Mode** In full duplex mode, GPSI_P5CRS reflects the receive carrier sense situation on medium only; In Half Duplex, GPSI_P5CRS will be high both in receive and transmit condition.
58	MII_P5COL	I	PD, LVTTL	**Port 5 Collision Input in MII Mode** Active high to indicate that there is a collision on the medium. Stay low in full duplex operation.
	GPSI_P5COL	I	PD, LVTTL	**Port 5 Collision Input in GPSI Mode** Active high to indicate that there is collision on the medium. Stay low in full duplex operation.
72	MII_P5RXCLK	I	PD, LVTTL	**Port 5 Receive Clock Input in MII Mode** MII_P5RXDV and MII_P5RXD[3:0] are synchronous to the rising edge of this clock. It is free running 25MHz clock in 100M mode and 2.5MHz clock in 10M mode.
	GPSI_P5RXCLK	I	PD, LVTTL	**Port 5 Receive Clock Input in GPSI Mode** GPSI_P5RXD are synchronous to the rising edge of this clock. It is non-continuous 10MHz Clock input.
67	MII_P5TXCLK	I	PD, LVTTL	**Port 5 Transmit Clock Input in MII Mode** MII_P5TXEN and MII_P5TXD[3:0] are output at the rising edge of this clock. It is free running 25MHz clock in 100M mode and 2.5MHz clock in 10M mode.
	GPSI_P5TXCLK	I	PD, LVTTL	**Port 5 Transmit Clock Input in GPSI Mode** GPSI_P5TXEN and GPSI_P5TXD are synchronous to the rising edge of this clock. It is continuous 10MHz Clock input.
89	SPDTNP5	I	PD, LVTTL	**Port 5 Speed Input** 0_B , 100M 1_B , 10M
90	LNKFP5	I	PD, LVTTL	**Port 5 Link Fail Status Input** 0_B , Link Up 1_B , Link Failed
91	DPHALFP5	I	PD, LVTTL	**Port 5 Duplex Status Input** 0_B , Full Duplex 1_B , Half Duplex
LED Interface				

Table 3 IO Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
107	DPHALFP4	I	PD, LVTTL	**Port 4 Duplex status Input** When Port 4 operates under MAC MII mode (see **CFG0** for more detail), this pins is used to select the duplex mode of Port 4. 0_B , Full Duplex 1_B , Half Duplex
	DUPCOL4	O	8 mA, PD, LVTTL	**Port 4 Duplex /Collision LED** When Port 4 operates under PHY or PCS MII mode (see **CFG0** for more details), in Full duplex mode, this pin acts as DUPLEX LED for Port 4; in half duplex mode, it is collision LED for each port. See **Chapter 3.20 LED Display** for more details.
110	DUPCOL3	O	8 mA, PD, LVTTL	**Port 3 Duplex /Collision LED** In Full duplex mode, this pin acts as DUPLEX LED for Port 3, respectively in half duplex mode, it is collision LED for each port. See **Chapter 3.20 LED Display** for more details.
111	BPEN	I	PU, LVTTL	**Recommend Back-Pressure in Half-Duplex** Value on this pin will be latched by ADM6996F during power on reset as the back-pressure enable in half-duplex mode. *Note: Power On Setting* 0_B , Disable Back-Pressure 1_B , Enable Back-Pressure
	DUPCOL2	O	8 mA, PU, LVTTL	**Port 2 Duplex-collision LED** In Full duplex mode, this pin acts as Port 2 DUPLEX LED; in half duplex mode, it is collision LED for Port 2. See **Chapter 3.20 LED Display** for more detail.
112	PHYAS1	I	PD, LVTTL	**Recommend PHY Address Bit 1** Value on this pin will be latched by ADM6996F during power on reset as the PHY address recommend value bit 1. See **PHYAS0** description for more details. *Note: Power On Setting*
	DUPCOL1	O	8 mA, PD, LVTTL	**Port 1 Duplex-collision LED** In Full duplex mode, this pin acts as port 1 DUPLEX LED; in half duplex mode, it is collision LED for Port 1. See **Chapter 3.20 LED Display** for more details.

Table 3 IO Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
113	RECANEN	I	PU, LVTTL	**Recommend Auto Negotiation Enable** Only valid for Twisted pair interface. Programming this bit to 1 has no effect to Fiber port. *Note: Power On Setting.* 0_B , Disable all TP port auto negotiation capability 1_B , Enable all TP port auto negotiation capability
	DUPCOL0	O	8 mA, PU, LVTTL	**Port 0 Duplex-collision LED** In Full duplex mode, this pin acts as port 0 DUPLEX LED; in half duplex mode, it is collision LED for Port 0. See **Chapter 3.20 LED Display** for more detail.
92	LNKFP4	I	PD, LVTTL	**Port 4 Link Fail Status Input** When Port 4 operates under MAC MII mode (see **CFG0** for more details), this pins is used as link control of Port 4. 0_B , Link Up 1_B , Link Failed
	LNKACT_4	O	8 mA, PD, LVTTL	**LINK/Activity LED of Port 4** When Port 4 operates under PHY or PCS MII mode (see **CFG0** for more details), this pin is used to indicate the link/activity status of Port 4, see **Chapter 3.20 LED Display** for more details.
95	LNKACT_3	O	8 mA, PD, LVTTL	**LINK/Activity LED of Port 3 to 0** Used to indicate corresponding port' s link/activity status, see **Chapter 3.20 LED Display** for more details.
96	LNKACT_2			
97	LNKACT_1			
98	LNKACT_0			
51	SPDTNP4	I	PD, LVTTL	**Port 4 Speed Input** When Port 4 operates under MAC MII mode (see **CFG0** for more details), this pin is used to select the operating speed of Port 4. 0_B , 100M 1_B , 10M
	LDSPD_4	O	8 mA, PD, LVTTL	**Port 4 Speed LED** When Port 4 operates under PHY or PCS MII mode (see **CFG0** for more details), this pin is used to indicate the speed status of Port 4, see **Chapter 3.20 LED Display** for more details.
48	LDSPD_3	O	8 mA, PD, LVTTL	**Port 3 to Port 0 Speed LED** Used to indicate corresponding port's speed status, see **Chapter 3.20 LED Display** for more details.
47	LDSPD_2			
43	LDSPD_1			
42	LDSPD_0			
EEPROM Interface				

Table 3 IO Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
84	EDO	I	PU, LVTTL	**EEPROM Data Output** This pin is used to input EEPROM data when reading EEPROM. During ADM6996F initialize itself, ADM6996F will drive EEPROM interface signal to read settings from EEPROM. Any other devices attached to EEPROM interface SHOULD drive Hi-Z or keep tristate during this period. See **Chapter 4.6 EEPROM Access** for more details.
80	IFSEL	I	PD, LVTTL	**Interface Selection** After the ADM6996F initialization process is done, this pin is used to select using EEPROM interface or SDC/SDIO interface. EECS/IFSEL interface 0_B , SDC/SDIO interface 1_B , EEPROM interface
	EECS	O	4 mA, PD, LVTTL	**EEPROM Chip Select** During the ADM6996F initialize itself, this pin is used as EEPROM chip select signal. During the ADM6996F initialize itself, ADM6996F will drive EEPROM interface signal to read settings from EEPROM. Any other devices attached to EEPROM interface SHOULD drive Hi-Z or keep tristate during this period. See **Chapter 4.6 EEPROM Access** for more details.
81	XOVEN	I	PD, LVTTL	**Cross Over Enable** Value on this pin (active low) will be latched by ADM6996F at the rising edge of RESETL(**RC**) for Port 4~0 crossover auto detect (Only available in TP interface). *Note: Power On Setting.* 0_B , Disable 1_B , Enable
	EESK	I/O	4 mA, PD, LVTTL	**EEPROM Serial Clock** During the ADM6996F initialize itself, this pin is used to output clock to EEPROM. After ADM6996F initialization process is done, this pin is used as EEPROM interface clock input if **IFSEL** = 1.
	SDC	I	PD, LVTTL	**Serial Management interface Clock input** If **IFSEL** = 0, this pin is used as serial management interface clock input.

Table 3 IO Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
79	LED_MODE	I	PD, LVTTL	**Enable Mac to Choose LED Display Mode** Value on this pin will be latched by ADM6996F at the rising edge of RESETL(**RC**) as single/dual color LED mode control signal. *Note: Power On Setting.* 0_B , Single color mode 1_B , Dual color mode
	EDI	I/O	8 mA, PD, LVTTL	**EEPROM Serial Data Input** During the ADM6996F initialize itself, this pin is used to output address and command to access EEPROM. After the initialization process is done, this pin becomes an input pin to monitor EEPROM data if **IFSEL** = 1.
	SDIO	I/O	8 mA, PD, LVTTL	**Serial Management interface Data input/Output** If **IFSEL** = 0, this pin is used as data input/output pin of serial management interface.
Power/Ground, 48 Pins				
4, 5, 12, 13, 20, 27, 28, 34, 35	GNDA	GND	–	**Ground** Used by AD Block
1, 9, 17, 24, 38	VCCA2	PWR	–	**1.8 V, Power** Used by TX Line Driver
8, 16, 23, 31	VCCAD	PWR	–	**3.3 V, Power** Used by AD Block
126	GNDBIAS	GND	–	**Ground** Used by Bias Block
128	VCCBIAS	PWR	–	**3.3 V, Power** Used by Bias Block.
123	GNDPLL	GND	–	**Ground** Used by PLL
122	VCCPLL	PWR	–	**1.8 V, Power** Used by PLL
45, 64, 76, 83, 93, 118	GNDIK	GND	–	**Ground** Used by Digital Core
46, 65, 75, 82, 94, 116	VCCIK	PWR	–	**1.8 V, Power** Used by Digital Core
50, 69, 70, 87, 99, 108	GNDO	GND	–	**Ground** Used by Digital Pad
49, 71, 88, 109	VCC3O	PWR	–	**3.3 V, Power** Used by Digital Pad
Miscellaneous				
41	TEST	I	PD, LVTTL	**Test Mode** Reserved and should keep 0 when normal operation.

Table 3 IO Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
86	CFG0	I	PU, LVTTL	**Configuration 0** Combined with **P4_BUSMD0** and **P4_BUSMD1**, ADM6996F provides 3 bus type for port 4. {CFG0, P4_BUSMD[1:0]}, Bus Mode of Port 4 0_00_B, PHY Interface 0_01_B, MAC MII 1_XX_B, PCS MII
40	MDIO	I/O	8 mA, PD, LVTTL	**Management Data** MDIO transfers management data in and out of the device synchronous to MDC.
44	MDC	I	PD, ST	**Management Data Reference Clock** A non-continuous clock input for management usage. ADM6996F will use this clock to sample data input on MDIO and drive data onto MDIO according to rising edge of this clock.
85	CKO25M	O	8 mA, PD, LVTTL	**25M Clock Output** Free Running 25M Clock output (Even during power on reset)
119	RC	I	ST	**RC Input For Power On Reset** This pin is sampled by using the 25MHz free running clock signal which input from **XI** to generate the low-active reset signal, RESETL. See **Chapter 5.3.2 Power On Reset** for the timing requirement.
120	XI	AI	ANA	**25MHz Crystal /Oscillator Input** 25MHz Crystal or Oscillator Input. Variation is limited to +/-50ppm.
121	XO	AO	ANA	**25MHz Crystal Output** When connected to oscillator, this pin should left unconnected.
127	RTX	AI	ANA	**Constant Voltage Reference** External 1.2 kΩ 1% resistor connection to ground.
125	VREF	AI	ANA	**Analog Reference Voltage** Used by Internal Bias Circuit for voltage reference.
124	CONTROL	AI/O	ANA	**FET Control Signal** The pin is used to control FET for 3.3 V to 1.8 V regulator.

3 Function Description

3.1 Functional Descriptions

The ADM6996F integrates five 100Base-X physical sub-layer (PHY), 100Base-TX physical medium dependent (PMD) transceivers, five complete 10Base-T modules, a 6 port 10/100 switch controller and one 10/100 MII/GPSI MAC and memory into a single chip for both 10Mbit/s, 100Mbit/s Ethernet switch operation. It also supports 100Base-FX operation through external fiber-optic transceivers. The device is capable of operating in either Full Duplex mode or Half-Duplex mode in 10Mbit/s and 100Mbit/s. Operational modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The ADM6996F consists of three major blocks:

- 10/100M PHY Block
- Switch Controller Block
- Built-in SSRAM

The interfaces used for communication between the PHY block and switch core is an MII interface.

An auto MDIX function is supported in this block. This function can be Enabled and Disabled by the hardware pin.

3.2 10/100M PHY Block

The 100Base-X section of the device implements the following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- Twisted-pair transceiver (PMD)

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

3.3 100Base-X Module

The ADM6996F implements a 100Base-X compliant PCS and PMA and 100Base-TX compliant TP-PMD. Bypass options for each of the major functional blocks within the 100Base-X PCS provides flexibility for various applications. 100Mbit/s PHY loop back is included for diagnostic purpose.

3.4 100Base-X Receiver

The 100Base-X receiver consists of functional blocks required to recover and condition the 125Mbit/s receive data stream. The ADM6996F implements the 100Base-X receiving state machine diagram as given in the ANSI/IEEE Standard 802.3u, Clause 24. The 125Mbit/s receive data stream may originate from the on-chip twisted-pair transceiver in a 100Base-TX application. Alternatively, the receive data stream may be generated by an external optical receiver as in a 100Base-FX application.

The receiver block consists of the following functional sub-blocks:

- A/D Converter
- Adaptive Equalizer and timing recovery module
- NRZI/NRZ and serial/parallel decoder
- De-scrambler
- Symbol alignment block
- Symbol Decoder
- Collision Detect Block

- Carrier sense Block
- Stream decoder block

3.4.1 A/D Converter

A high performance A/D converter with a 125Mhz sampling rate converts signals received on the RXP/RXN pins to 6 bits data streams. It possesses an auto-gain-control capability that will further improve receive performance especially under long cabling or harsh detrimental signal integrity. Due to high pass characteristic on a transformer, a built in base-line-wander correcting circuit will be cancelled out and its DC level restored.

3.4.2 Adaptive Equalizer and timing Recovery Module

All digital design is especially immune to noise environments and achieves better correlation between production and system testing. Baud rate Adaptive Equalizer/Timing Recovery compensates for line loss induced from twisted pairs and tracks a far end clock at 125M samples per second. Adaptive Equalizer's implemented with Feed forward and Decision Feedback techniques meet the requirement of BER with less than 10-12 for transmission on a CAT5 twisted pair cable ranging from 0 to 120 meters.

3.4.3 NRZI/NRZ and Serial/Parallel Decoder

The recovered data is converted from NRZI to NRZ. The data is not necessarily aligned to the 4B/5B code group's boundary.

3.4.4 Data De-scrambling

The de-scrambler acquires synchronization with the data stream by recognizing idle bursts of 40 or more bits and locking its deciphering Linear Feedback Shift Register (LFSR) to the state of the scrambling LFSR. Upon achieving synchronization, the incoming data is XORed by the deciphering LFSR and de-scrambled.

In order to maintain synchronization, the de-scrambler continuously monitors the validity of the unscrambled data that it generates. To ensure this, a link state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the de-scrambler the hold timer starts a 722 micro second countdown. Upon detection of sufficient idle symbols within the 722 micro sec. period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given an operating network connection operating with good signal integrity. If the link state monitor does not recognize sufficient unscrambled idle symbols within the 722 micro second period, the de-scrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization.

3.4.5 Symbol Alignment

The symbol alignment circuit in the ADM6996F determines code word alignment by recognizing the /J/K delimiter pair. This circuit operates on unaligned data from the de-scrambler. Once the /J/K symbol pair (11000 10001_B) is detected, subsequent data is aligned on a fixed boundary.

3.4.6 Symbol Decoding

The symbol decoder functions is a look-up table that translates incoming 5B symbols into 4B nibbles. The symbol decoder first detects the /J/K symbol pair preceded by idle symbols and replaces the symbol with a MAC preamble. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R symbol pair denoting the end of stream delimiter (ESD). The translated data is presented on the internal RXD[3:0] signal lines where RXD[0] represents the least significant bit of the translated nibble.

3.4.7 Valid Data Signal

The valid data signal (RXDV) indicates that recovered and decoded nibbles are being presented on the internal RXD[3:0] synchronous receive clock, RXCLK. RXDV is asserted when the first nibble of a translated /J/K is ready for transfer over the internal MII. It remains active until either the /T/R delimiter is recognized, link test indicates failure, or no signal is detected. On any of these conditions, RXDV is de-asserted.

3.4.8 Receive Errors

The RXER signal is used to communicate receiver error conditions. While the receiver is in a state of holding RXDV asserted, the RXER will be asserted for each code word that does not map to a valid code-group.

3.4.9 100Base-X Link Monitor

The 100Base-X link monitor function allows the receiver to ensure that reliable data is being received. Without reliable data reception, the link monitor will halt both transmit and receive operations until such time that a valid link is detected.

The ADM6996F performs the link integrity test as outlined in IEEE 100Base-X (Clause 24) link monitor state diagram. The link status is multiplexed with 10Mb/s link status to form the reportable link status bit in the serial management register 1h, and driven to the LNKACT pin.

When persistent signal energy is detected on the network, the logic moves into a Link-Ready state after approximately 500 micro secs, and waits for an enable from the auto negotiation module. When received, the link-up state is entered, and the transmission and reception logic blocks become active. Should auto negotiation be disabled, the link integrity logic moves immediately to the link-up state after entering the link-ready state.

3.4.10 Carrier Sense

Carrier sense (CRS) for 100Mbit/s operation is asserted upon the detection of two non contiguous zeros occurring within any 10-bit boundary of the received data stream.

The carrier sense function is independent of symbol alignment. In switch mode, CRS is asserted during either packet transmission or reception. For repeater mode, CRS is asserted only during packet reception. When the idle symbol pair is detected in the received data stream, CRS is de-asserted. In repeater mode, CRS is only asserted due to receive activity. CRS is intended to encapsulate RXDV.

3.4.11 Bad SSD Detection

A Bad Start of Stream Delimiter (Bad SSD) is an error condition that occurs in the 100Base-X receiver if a carrier is detected (CRS asserted) and a valid /J/K set of code-group (SSD) is not received.

If this condition is detected, then the ADM6996F will assert RXER and present RXD[3:0] = 1110_B to the internal MII for the cycles that correspond to received 5B code-groups until at least two idle code-groups are detected. Once at least two idle code groups are detected, RXER and CRS become de-asserted.

3.4.12 Far-End Fault

Auto negotiation provides a mechanism for transferring information from the Local Station to the link Partner that a remote fault has occurred for 100Base-TX. As auto negotiation is not currently specified for operation over fiber, the far end fault indication function (FEFI) provides this capability for 100Base-FX applications.

A remote fault is an error in the link that one station can detect while the other cannot. An example of this is a disconnected wire at a station's transmitter. This station will receive the valid data and detect if the link is good via the link integrity monitor, but will not be able to detect if its transmission is not propagating to the other station.

A 100Base-FX station that detects such a remote fault may modify its transmitted idle stream from all 1_B's to a group of 84 1_B's followed by a single 0_B. This is referred to as the FEFI idle pattern.

3.5 100Base-TX Transceiver

The ADM6996F implements a TP-PMD compliant transceiver for 100Base-TX operation. The differential transmit driver is shared by the 10Base-T and 100Base-TX subsystems. This arrangement results in one device that uses the same external magnetic for both the 10Base-T and the 100Base-TX transmissions with a simple RC component connection. The individually wave-shaped 10Base-T and 100Base-TX transmit signals are multiplexed in the transmission output driver selection.

3.5.1 Transmit Drivers

The ADM6996F 100Base-TX transmission driver implements MLT-3 translation and wave-shaping functions. The rise/fall time of the output signal is closely controlled to conform to the target range as specified in the ANSI TP-PMD standard.

3.5.2 Twisted-Pair Receiver

For 100Base-TX operation, the incoming signal is detected by the on-chip twisted-pair receiver that consists of a differential line receiver, an adaptive equalizer and a base-line wander compensation circuits.

The ADM6996F uses an adaptive equalizer that changes filter frequency response in accordance with cable length. The cable length is estimated based on the incoming signal strength. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions incurred from the cable.

3.6 10Base-T Module

The 10Base-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loop back, jabber, wave shaper, and link integrity functions, as defined in the standard.

The ADM6996F 10Base-T module is comprised of the following functional blocks:

- Manchester encoder and decoder
- Collision detector
- Link test function
- Transmit driver and receiver
- Serial and parallel interface
- Jabber and SQE test functions
- Polarity detection and correction

3.6.1 Operation Modes

The ADM6996F 10Base-T module is capable of operating in either half-duplex mode or full-duplex mode. In half-duplex mode, the ADM6996F functions as an IEEE 802.3 compliant transceiver with fully integrated filtering. The COL signal is asserted during collisions or jabber events, and the CRS signal is asserted during transmit and receive. In full duplex mode the ADM6996F can simultaneously transmit and receive data.

3.6.2 Manchester Encoder/Decoder

Data encoding and transmission begins when the transmission enable input (TXEN) goes high and continues as long as the transceiver is in a good link state. Transmission ends when the transmission enable input goes low. The last transition occurs at the center of the bit cell if the last bit is a 1_B, or at the boundary of the bit cell if the last bit is 0_B.

Decoding is accomplished using a differential input receiver circuit and a phase-locked loop that separate the Manchester-encoded data stream into clock signals and NRZ data. The decoder detects the end of a frame when no more mid bit transitions are detected. Within one and a half bit times after the last bit, carrier sense is de-asserted.

3.6.3 Transmit Driver and Receiver

The ADM6996F integrates all the required signal conditioning functions in its 10Base-T block such that external filters are not required. Only one isolation transformer and impedance matching resistors are needed for the 10Base-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmission signal are attenuated properly.

3.6.4 Smart Squelch

The smart squelch circuit is responsible for determining when valid data is present on the differential receive. The ADM6996F implements an intelligent receive squelch on the RXP/RXN differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of the packet is checked by the analog squelch circuit and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150ns. Finally, the signal must exceed the original squelch level within an additional 150ns to ensure that the input waveform will not be rejected.

Only after all these conditions have been satisfied a control signal will be generated to indicate to the remainder of the circuitry that valid data is present.

Valid data is considered to be present until the squelch level has not been generated for a time longer than 200 ns, indicating the end of a packet. Once good data has been detected, the squelch levels are reduced to minimize the effect of noise, causing premature end-of-packet detection. The receive squelch threshold level can be lowered for use in longer cable applications. This is achieved by setting bit 10 of register address 11_H.

3.7 Carrier Sense

Carrier Sense (CRS) is asserted due to receive activity once valid data is detected via the smart squelch function. For 10 Mbit/s half duplex operation, CRS is asserted during either packet transmission or reception. For 10 Mbit/s full duplex and repeater mode operations, the CRS is asserted only due to receive activity.

3.8 Jabber Function

The jabber function monitors the ADM6996F output and disables the transmitter if it attempts to transmit a longer than legal sized packet. If TXEN is high for greater than 24ms, the 10Base-T transmitter will be disabled. Once disabled by the jabber function, the transmitter stays disabled for the entire time that the TXEN signal is asserted. This signal has to be de-asserted for approximately 256 ms (the un-jab time) before the jabber function re-enables the transmit outputs. The jabber function can be disabled by programming bit 4 of register address 10_H to high.

3.9 Link Test Function

A link pulse is used to check the integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted-pair transmitter, receiver, and collision detection functions.

The link pulse generator produces pulses as defined in IEEE 802.3 10Base-T standard. Each link pulse is nominally 100ns in duration and is transmitted every 16 ms, in the absence of transmit data.

3.10 Automatic Link Polarity Detection

The ADM6996F's 10Base-T transceiver module incorporates an "automatic link polarity detection circuit". The inverted polarity is determined when seven consecutive link pulses of inverted polarity or three consecutive packets are received with inverted end-of-packet pulses. If the input polarity is reversed, the error condition will be automatically corrected and reported in bit 5 of register 10_H.

3.11 Clock Synthesizer

The ADM6996F implements a clock synthesizer that generates all the reference clocks needed from a single external frequency source. The clock source must be a TTL level signal at 25 MHz +/- 50ppm

3.12 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further details regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The ADM6996F supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

Highest priority is relative to the following list:

- 100Base-TX full duplex (highest priority)
- 100Base-TX half duplex
- 10Base-T full duplex
- 10Base-T half duplex (lowest priority)

3.13 Memory Block

The ADM6996F's built in memory is divided into two blocks. One is a MAC addressing table and the other one is a data buffer.

The MAC address Learning Table size has 2K entries with each entry occupying eight bytes length. These eight bytes of data include a 6 byte source address, VLAN information, Port information and an aging counter.

A data buffer is divided into 256 bytes/block. The ADM6996F buffer management is per port fixed block number and all ports share one global buffer. This architecture can get better memory utilization and network balance at different speeds and duplex test conditions.

Received packets will be separated into several 256 bytes/block and chain together. If a packet size is more than 256 bytes then the ADM6996F will chain two or more blocks to store receiving packets.

3.14 Switch Functional Description

The ADM6996F uses a "store & forward" switching approach for the following reason:

- Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require large elastic buffers especially when bridging between a server on a 100 Mbit/s network and clients on a 10 Mbit/s segment.
- Store & forward switches improve overall network performance by acting as a "network cache"
- Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port.

3.15 Basic Operation

The ADM6996F receives incoming packets from one of its ports, searches in the Address Table for the Destination MAC Address and then forwards the packet to the other port within the same VLAN group, where appropriate. If the destination address is not found in the address table, the ADM6996F treats the packet as a broadcast packet and forwards the packet to the other ports within the same VLAN group.

The ADM6996F automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets at wire speed. If the Source Address is not found in the Address Table, the device adds it to the table.

3.15.1 Address Learning

A one-way hash algorithm is implemented to allow the maximum of 1 different addresses with the same hash key to be stored at the same time. Up to 2K entries can be created and all entries are stored in the internal SSRAM. An address is stored in the Address Table. The ADM6996F searches for the Source Address (SA) of an incoming packet in the Address Table and acts as below:

1. If the SA was not found in the Address Table (a new address), the ADM6996F waits until the end of the packet (non-error packet) and updates the Address Table. If the SA was found in the Address Table, then the aging value of each corresponding entry will be reset to 0_B.
2. When the DA is PAUSE command, then the learning process will be disabled automatically by ADM6996F.

3.15.2 Address Recognition and Packet Forwarding

The ADM6996F forwards the incoming packets between bridged ports according to the Destination Address (DA) as below. All the packets forwarded will check the VLAN first. A forwarding port must be within the same VLAN as the source port.

If the DA is a UNICAST address and the address was found in the Address Table, the ADM6996F will check the port number and act as follows:

- If the port number is equal to the port on which the packet was received, the packet is discarded.
- If the port number is different, the packet is forwarded across the bridge.
- If the DA is a UNICAST address and the address was not found, the ADM6996F treats it as a multicast packet and forwards it across the bridge.
- If the DA is a Multicast address, the packet is forwarded across the bridge.
- If the DA is a PAUSE Command (01 80 C2 00 00 01_H), then this packet will be dropped by the ADM6996F. The ADM6996F can issue and learn PAUSE commands.
- The ADM6996F will forward the packet with a DA of (01 80 C2 00 00 00_H), filter out the packet with a DA of (01 80 C2 00 00 01_H), and forward a packet with a DA of (01-80-C2-00-00-02_H to 01 80 C2 00 00 $0F_H$)

3.15.3 Address Aging

Address aging is supported for topology changes such as an address moving from one port to another. When this happens, the ADM6996F internally has a 300 second timer which will “age-out” (remove) the address from the address table. The aging function can be enabled/disabled by the user. Normally, disabling an aging function is for security purposes.

3.15.4 Back off Algorithm

The ADM6996F implements the truncated exponential back off algorithm compliant to the 802.3 CSMA-CD standard. The ADM6996F will restart the back off algorithm by choosing 0-9 collision counts. The ADM6996F resets the collision counter after 16 consecutive retransmit trials.

3.15.5 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The typical number is 96 bits at a time. The value is 9.6 micro secs for 10 Mbit/s Ethernet, 960ns for 100 Mbit/s fast Ethernet. The ADM6996F provides an option of average 92 bit gap in an EEPROM register to shorten the IPG.

3.15.6 Illegal Frames

The ADM6996F will discard all illegal frames such as small packets (less than 64 bytes), oversized packets (greater than 1518 or 1522 bytes) and bad CRC. Dribbling packing with good CRC value will be accepted by the ADM6996F. In case of bypass mode enable, the ADM6996F will support tagged and untagged packets with sizes

up to 1522 bytes. In case of non-bypass mode, the ADM6996F will support tagged packets up to 1526bytes and untagged packets up to 1522bytes.

3.15.7 Half Duplex Flow Control

A back pressure function is supported for half-duplex operations. When the ADM6996F cannot allocate a receive buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision. Back Pressure is enabled by the BPEN set during RESET assertion. An Infineon proprietary algorithm is implemented inside the ADM6996F to prevent the back pressure function causing HUB partitioned under heavy traffic environment and reducing the packet loss rate to increase the whole system performance.

3.15.8 Full Duplex Flow Control

When full duplex port runs out of its receive buffer space, a PAUSE packet command will be issued by ADM6996F to notice the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. ADM6996F can issue or receive pause packet.

3.15.9 Broadcast Storm filter

If the Broadcast Storm filter is enabled, the broadcast packets over 50 ms of the threshold will be discarded by the threshold setting. See EEPROM Reg.10_H.

Broadcast storm mode:

Time interval : 50ms

Max. packet number = 7490 in 100Base, 749 in 10Base

Table 4 The max. packet number = 7490 in 100Base, 749 in 10Base

Per Port Falling Threshold				
	00_B	01_B	10_B	11_B
All 100TX	Disable	5%	10%	20%
Not All 100TX	Disable	0.5%	1%	2%

Table 5 The max. packet number = 7490 in 100Base, 749 in 10Base

Per Port Rising Threshold				
	00_B	01_B	10_B	11_B
All 100TX	Disable	10%	20%	40%
Not All 100TX	Disable	1%	2%	4%

3.16 Auto TP MDIX Function

In normal applications with the Switch connected to a NIC card it uses one by one TP cable. If Switch connects another device such as another Switch, then (it) must by two way. First one is Cross Over TP cable and second one is to use extra RJ45 which crossover internal TX+- and RX+- signal. By second way customer can use one by one cable to connect two Switch devices. All these efforts cause extra costs and is not a good solution. ADM6996F provides Auto MDIX function which can adjust TX+- and RX+- at correct pin. User can use one by one cable between ADM6996F and another device. This function can be Enable/Disable by hardware pin and EEPROM configuration register 01_H ~ 09_H bit 15. If hardware pin sets all ports at Auto MDIX mode then EEPROM setting is useless. If hardware pin sets all ports at non Auto MDIX mode then EEPROM can set each port of this function enable or disable.

3.17 Port Locking

Port locking function will provide customer a simple way to limit per port user number to one. If this function is turned on then the ADM6996F will lock first MAC address in learning table. After this MAC address locking will never age out except Reset signal. Another MAC address which is not the same as the locked one will be dropped. ADM6996F provides one MAC address per port. This function is per port setting. When turned on Port Locking function, recommend customer turns off aging function. See EEPROM register 12_H bit 0~8.

3.18 VLAN setting & Tag/Untag & port-base VLAN

ADM6996F supports bypass mode and untagged port as default setting while the chip is power-on. Thus, every packet with or without tag will be forwarding to the destination port without any modification by ADM6996F. Meanwhile port-base VLAN could be enabled according to the PVID value (user define 4bits to map 16 groups written at register 13_H to register 22_H) of the configuration content of each port.

ADM6996F also supports 16 802.1Q VLAN groups. In VLAN four bytes tags include twelve VLAN ID. ADM6996F lets user define four bits of VID. If user need to use this function, two EEPROM registers are needed to be programmed first:

* Port VID number at EEPROM register 01_H ~ 09_H bit 13~10, register 28_H ~ $2B_H$ and register $2C_H$ bit 7~0: ADM6996F will check coming packet. If coming packet is non VLAN packet then ADM6996F will use PVID as VLAN group reference. ADM6996F will use packet's VLAN value when receive tagged packet.

* VLAN Group Mapping Register. EEPROM register 13_H ~ 22_H define VLAN grouping value. User use these register to define VLAN group.

User can define each port as Tag port or Untag port by Configuration register Bit 4. The operation of packet between Tag port and Untag port can be explained by following example:

Example 1: Port receives Untag packet and send to Untag port.

ADM6996F will check the port user defined four bits of VLAN ID first then check VLAN group resister. If the destination port is the same VLAN as the receiving port then this packet will forward to destination port without any change. If the destination port is not the same VLAN as the receiving port then this packet will be dropped.

Example 2: Port receives Untag packet and send to Tag port.

ADM6996F will check the port user define fours bits of VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port with four byte VLAN Tag and new CRC. If destination port not same VLAN as receiving port then this packet will be dropped.

Example 3: Port receives Tag packet and send to Untag port.

ADM6996F will check the packet VLAN ID first then check VLAN group register. If the destination port is the same VLAN as the receiving port than this packet will forward to destination port after removing four bytes with new CRC error. If the destination port is not the same VLAN as the receiving port then this packet will be dropped.

Example 4: Port receives Tag packet and send to Tag port.

ADM6996F will check the user define packet VLAN ID first then check VLAN group register. If the destination port is the same VLAN as the receiving port than this packet will forward to destination port without any change. If destination port is not the same VLAN as the receiving port then this packet will be dropped.

3.19 Priority Setting

It is a trend that data, voice and video will be put on networking.A Switch does not only deal with data packets but also provides service of multimedia data. ADM6996F provides two priority queues on each port with N:1 rate. See EEPROM Reg.10_H.

This priority function can set three ways as below:

* By Port Base: Set specific port at specific queue. ADM6996F only check the port priority and does not check packet's content VLAN and TOS.

* By VLAN first: ADM6996F check VLAN three priority bit first then IP TOS priority bits.

* By IP TOS first: ADM6996F check IP TOS three priority bit first then VLAN three priority bits.

If port set at VLAN/TOS priority but the receiving packet is without VLAN or TOS information then port base priority will be used.

3.20 LED Display

Three LED per port are provided by ADM6996F. Link/Act, Duplex/Col. & Speed are three LED displays of ADM6996F. Dual color LED mode is also supported by ADM6996F. For easy production purpose ADM6996F will send test signal to each LED at power on reset stage. EEPROM register 12_H define LED configuration table.

1. **DXCL** (see 0012H): Dupcol LEDs indicate the duplex status only.
2. **DHCOL** (See 0030H): When enabled, pin DUPCOL0 shows col_10m status and pin DUPCOL1 shows col_100m status. These two LEDs are necessary in the dual-speed hub.

ADM6996F LED is active Low signal. Dupcol0 & Dupcol1 will check external signals at Reset. If external signal adds pull high then LED will be active Low. If external signal adds pull down resister then LED will drive high.

3.20.1 Single Color LED Display

Table 6 Single Color LED Display

Pin Name	Status
LNKACT4/LNKACT3/ LNKACT2/LNKACT1/ LNKACT0	These pins have no power-on reset values on them, and ADM6996F uses active low values to drive the LED. So the output values of these pins after the power on reset are shown as follows: 1. First period: This period lasts 1.28 s for LED on test. ADM6996F drives value 0 to open the LED. 2. Second period: This period lasts 0.48s for LED off test. ADM6996F drives value 1 to close the LED. 3. Normal Period: This period indicates the link status. 0B , Port links up and LED is ON. 1B , Port links down and LED is OFF. 0/1B , Port links up and is transmitting or receiving. The LED flashes at 10 Hz.
LDSPD4/LDSPD3/ LDSPD2/LDSPD1/ LDSPD0	The behavior of these pins is the same as the LNKACT, except in the normal period. Normal period: This period indicates the speed status. 0B , Port links up and its speed is 100M. LED is ON. 1B , Port links down or its speed is 10M. LED is OFF.

Table 6 Single Color LED Display (cont'd)

Pin Name	Status
DUPCOL2/ DUPCOL1/ DUPCOL0	These 3 pins have power-on reset values on them. ADM6996F needs to consider these values to drive the correct value. If the power on reset value is value_power_on, then the display is as follows: 1. First period: This period lasts 1.28s for LED on test. ADM6996F drives ~value_power_on to open the LED. 2. Second period: This period lasts 0.48s for LED off test. ADM6996F drives value_power_on to close the LED. 3. Normal Period: This period indicates the duplex/collision status. ~value_power_on = Port links up in the full-duplex mode. LED is ON. value_power_on = Port links down. LED flashes at 10 Hz. 0/1B , Port links up and collision is detected. The LED flashes at 10 Hz. If **DXCL** is enabled, the normal period changes its way to display. ~value_power_on = Port links up in the duplex mode. LED is ON. value_power_on = Port links down or links up in the half-duplex mode. LED is OFF. 0/1B , This value is cancelled. LED doesn't blink. If **DHCOL** is enabled, the display in the normal period is as follows: DUPCOL0: 10m collision indicator. 0/1B , One of the ports links up in 10M half-duplex mode and detects a collision event. The LED flashes at 20 Hz. value_power_on = When the above event is not satisfied, the LED is OFF. DUPCOL1: 100m collision indicator. 0/1B , One of the ports links up in 100M half-duplex mode and detects a collision event. The LED flashes at 20 Hz. value_power_on = The above event is not satisfied. LED is OFF.
DUPCOL4/ DUPCOL3	The behavior of these pins is the same as the LNKACT, except in the normal period. Normal period: This period indicates the duplex/collision status. ~value_power_on = Port links up in the full-duplex mode. LED is ON. value_power_on = Port links down. LED is OFF. 0/1B , Port links up and collision is detected. The LED flashes at 10 Hz. If **DXCL** is enabled, the normal period changes its way to display. ~value_power_on = Port links up in the duplex mode. LED is ON. value_power_on = Port links down or links up in the half-duplex mode. LED is OFF. 0/1B , This value is cancelled. LED doesn't blink.

3.20.2 Dual Color LED Display

Users should be careful that DUPCOL LED only supports single color mode. The only difference between single and dual color for DUPCOL LED is the self-test time.

Table 7 Dual Color LED Display

Pin Name	Status
(LNKACT4, LDSPD4)/ (LNKACT3, LDSPD3) (LNKACT2, LDSPD2) (LNKACT1, LDSPD1) (LNKACT0, LDSPD0)	First Period: Test LED is on with green color. It lasts 1.28s. 01B , LED is on with green color. Second Period: Test LED is on with yellow color. It lasts 1.28s. 10B , LED is on with yellow color. Third period: Test LED off. 00B , LED is off. Normal Period: This period shows the status of the link and speed at the same time. 00B , Port links down.LED is off. 11B , Port links down. LED is off. 01B , Port links up in 100M. LED glows green. 10B , Port links up in 10M. LED glows yellow. 0/1,1B , Port links up in 100M and is receiving or transmitting. LED blinks with green color at 10 Hz. 0/1,0B , Port links up in 10M and is receiving or transmitting. LED blinks with yellow color at 10 Hz.
DUPCOL4/DUPCOL3/ DUPCOL2/DUPCOL1/ DUPCOL0	The behavior of these pins is the same as in the single mode, except in the self-test period. The LED on test period is 2.56 s instead of 1.28 s.

3.20.3 Circuit for Single LED Mode

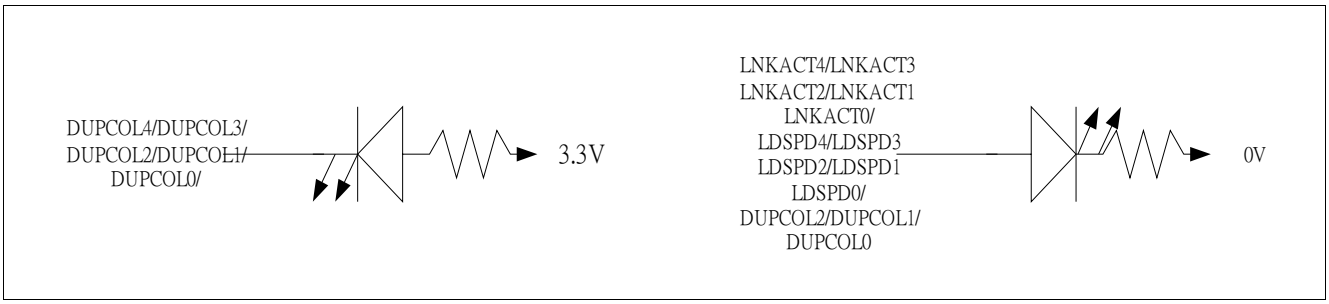


Figure 3 Circuit for Single Color LED Mode

3.20.4 Circuit for Dual Led Mode

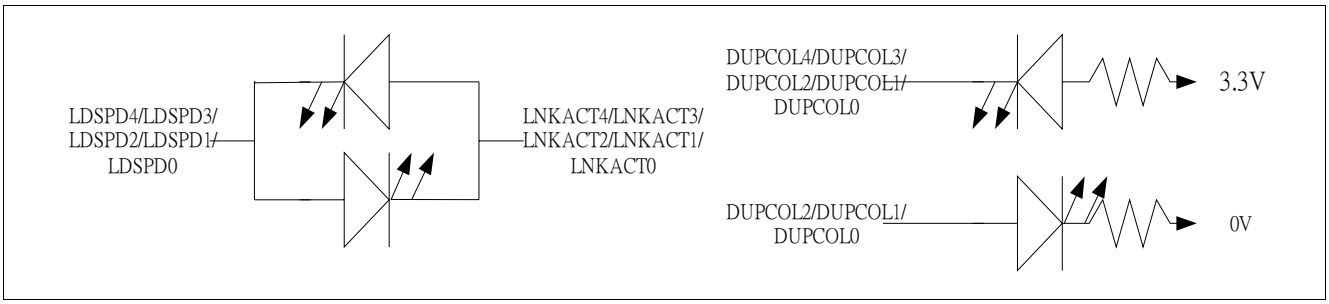


Figure 4 Circuit for Dual Color LED Mode

3.21 Port4 and Port5 MII connection

In ADM6996F, there are 3 different configurations (Normal PHY, MAC type MII and PCS type MII, **CFG0**) for Port4. If Port4 is configured in normal PHY mode, then it is identical to Port0~Port3 and Port4's MII signals are ignored. If Port4 is configured in MAC type MII mode, it can be used for HomePNA applications and the embedded single PHY will not be used. In ADM6996F, the most popular is to configure Port4 as the PCS type MII for a router's WAN port application. Users can see **Figure 5** and **Figure 6** to get a clearer picture. For Port5, there are two different configurations (MAC type MII mode and GPSI mode, **P5_GPSI**) for connecting to a CPU's MII/GPSI interface.

Here we dipict two general router applications of ADM6996F, one is connected to a CPU with a single MII and another is connected to a CPU with dual MII. In **Figure 5**, we can see whether LAN to WAN or WAN to LAN, the packets will go through the same MII port. Because the CPU needs to send out the packets with the registered MAC ID to the WAN port, this MAC ID may also come in from the LAN ports. We know the switch learning scheme can't permit packets with the same MAC ID input from different ports. In the ADM6996F design, we use the MAC clone and VLAN group to solve this problem. The **VLAN mode select Register**, provides users with more details for this implementation.

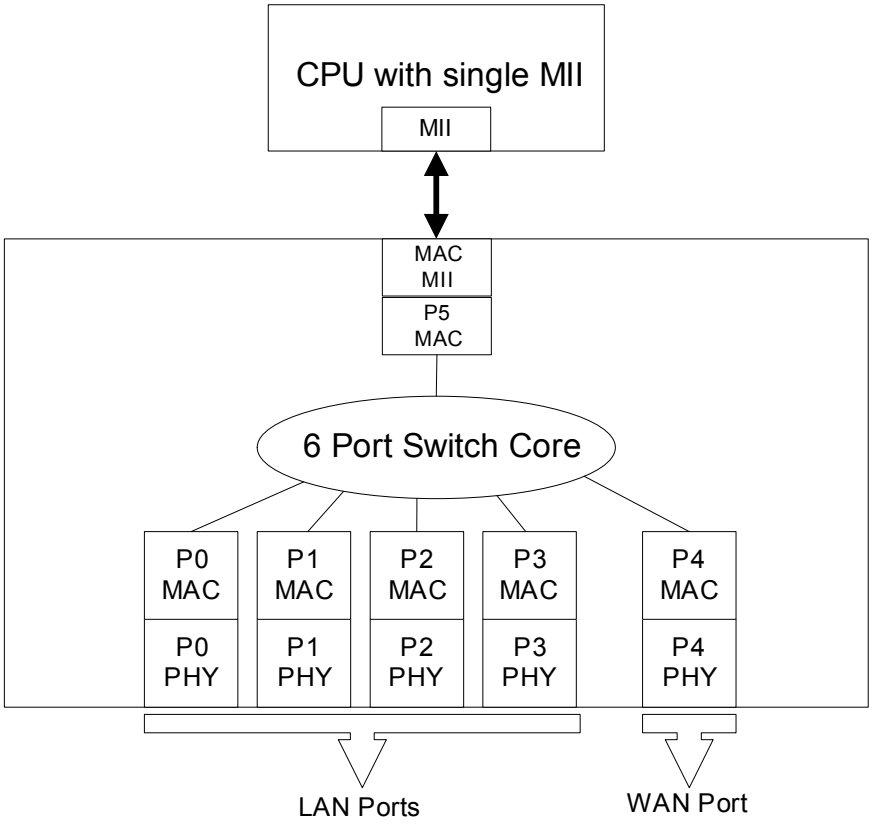


Figure 5 ADM6996F to CPU with single MII connection

Figure 6 shows an easy way to connect the CPU with dual MII for a routing application. In this application, Port4's embedded and isolated PHY will be connected to the WAN port. The CPU will act as the bridge to translate the packet's frame for LAN/WAN and use different MII to handle the packets either from LAN to WAN or from WAN to LAN. The isolated PHY is helpful to reduce the BOM cost.

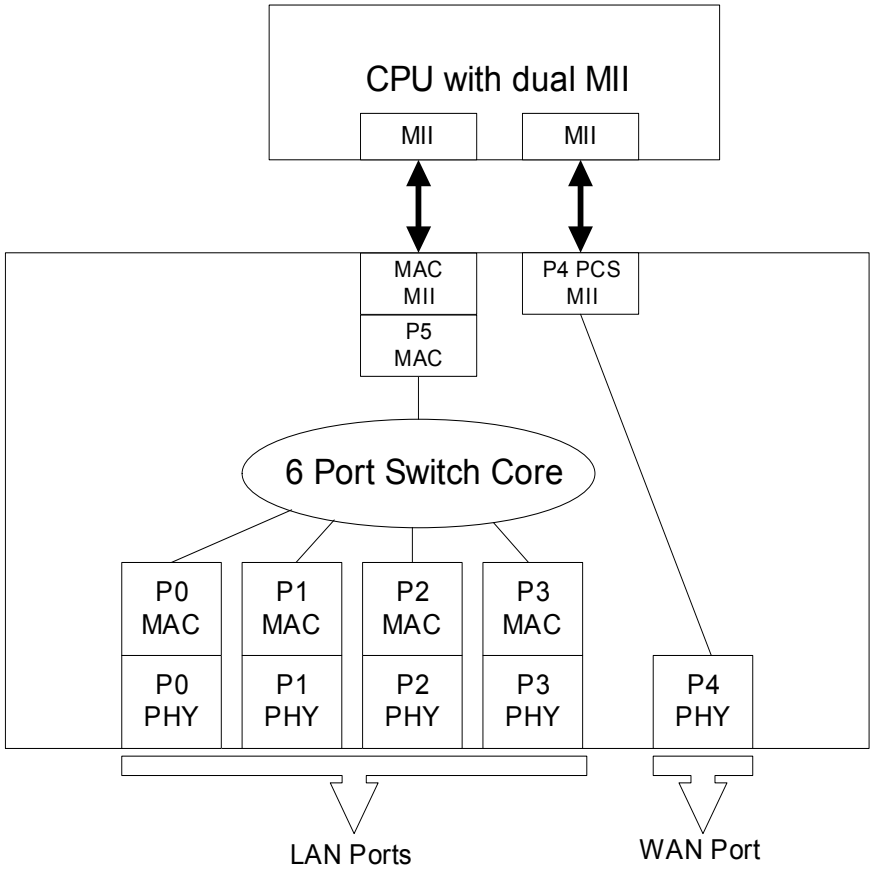


Figure 6 ADM6996F to CPU with dual MII connection

Normally, the MAC mode MII should be connected to the PCS mode MII. But in some applications, we need to connect both MACs mode MII to each other as shown in above figures. In Figure 6, due to most CPU's MII being MAC mode, Port4 is PCS to MAC connection and Port5 is MAC to MAC connection.

Through the hardware setting, it is easy to set ADM6996F Port5 MII to operate in 100M Full duplex mode. And this kind of mode (100M Full) is normally the operation mode to be with CPU, the interface connection is described in the following diagram.

(1) CKO25M is the 25M clock driven out by ADM6996F to fit 100M MII operation. This clock output provides 8mA driving capability and it can be connected directly to TXCLK/RXCLK.

(2) Due to it's Full Duplex operation mode,COL is tied to GND.

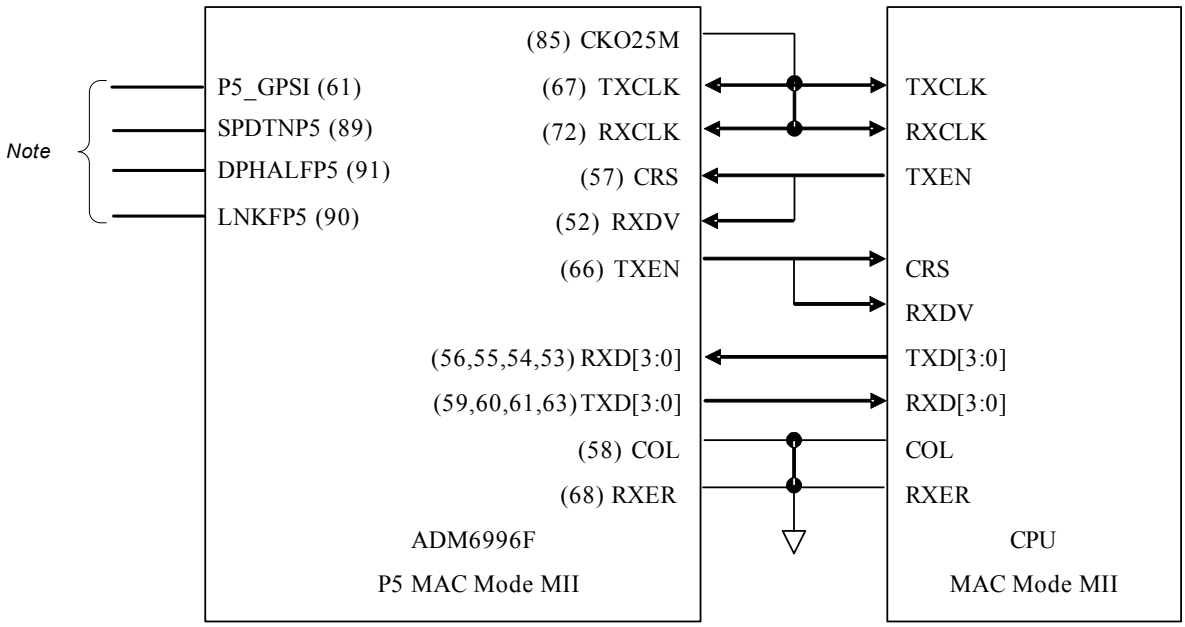


Figure 7 100M Full duplex MAC to MAC MII connection

Note:

1. *Pin 61 should be pull low to let P5_GPSI be latched as "0" and make Port5 operate in MII mode*
2. *Pin 89 (SPDTNP5) should be pull low or floating to set Port5 to 100Mbit/s.*
3. *Pin 91 (DPHALFP5) should be pull low or floating to set Port5 in full duplex mode.*
4. *Pin 90 (LNKFP5) should be pull low or floating to set Port5 Link up.*

The PCS mode MII connection to MAC mode MII is very straightforward. If PCS and MAC fto ollow the MII standard timing and users notice the PCB layout balance, it should not be an issue for PCS to connect the MAC. In **Figure 8**, we depict this interface connection and describe how to configure Port4 as the PCS mode MII.

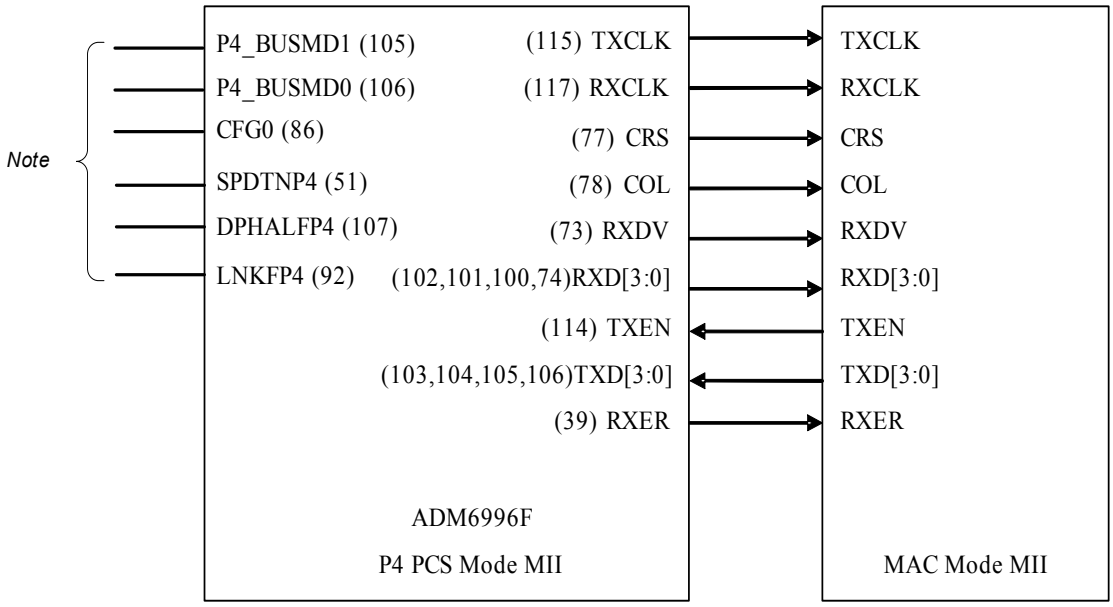


Figure 8 PCS to MAC MII connection

Note:

5. *From **CFG0**'s pin description, we know it needs to set {CFG0, P4_BUSMD[1:0]} as $1xx_B$ to configure Port4 in PCS mode MII. So it doesn't matter the value on P4_BUSMD[1:0] (pin 105 and pin 106) and we only pull high the CFG0 or make it floating (due to it having internal pull high).*
6. *Pin 51 (SPDTNP4) should be pull low or floating to set Port4's speed to 100Mbit/s and pull high to set speed to 10Mbit/s.*
7. *Pin 107 (DPHALFP4) should be pull low or floating to set Port4 in full duplex mode and pull high to set in half duplex mode.*
8. *Pin 92 (LNKFP4) should be pull low or floating to set Port4 link up and pull high to set link failed.*

4 Registers Description

4.1 EEPROM Registers

Table 8 Registers Address Space

Module	Base Address	End Address	Note
EEPROM	00_H	33_H	Independent Address Space

Table 9 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
SigReg	Signature Register	00_H	**42**
CtrlReg_0	Basic Control Register 0	01_H	**43**
ResReg_0	Reserved Register 0	02_H	**44**
CtrlReg_P1	Basic Control Register 1	03_H	**44**
ResReg_1	Reserved Register 1	04_H	**44**
CtrlReg_P2	Basic Control Register 2	05_H	**44**
ResReg_2	Reserved Register 2	06_H	**44**
CtrlReg_P3	Basic Control Register 3	07_H	**44**
CtrlReg_P4	Basic Control Register 4	08_H	**44**
ResReg_3	Reserved Register 3	09_H	**44**
ResReg_4	Reserved Register 4	$0A_H$	**45**
ConfigReg_1	Configuration Register 1	$0B_H$	**45**
ResReg_5	Reserved Register 5	$0C_H$	**45**
ResReg_6	Reserved Register 6	$0D_H$	**46**
VLAN_Map_P	VLAN priority Map Register	$0E_H$	**46**
TOS_Priority	TOS priority Map Register	$0F_H$	**47**
ConfigReg_2	Configuration Register 2	10_H	**47**
VLAN_Mode	VLAN Mode Select Register	11_H	**48**
ConfigReg_3	Miscellaneous Configuration Register 3	12_H	**51**
VLAN_Map_0	VLAN mapping table registers 0	13_H	**52**
VLAN_Map_1	VLAN mapping table registers 1	14_H	**53**
VLAN_Map_2	VLAN mapping table registers 2	15_H	**53**
VLAN_Map_3	VLAN mapping table registers 3	16_H	**53**
VLAN_Map_4	VLAN mapping table registers 4	17_H	**53**
VLAN_Map_5	VLAN mapping table registers 5	18_H	**53**
VLAN_Map_6	VLAN mapping table registers 6	19_H	**53**
VLAN_Map_7	VLAN mapping table registers 7	$1A_H$	**53**
VLAN_Map_8	VLAN mapping table registers 8	$1B_H$	**53**
VLAN_Map_9	VLAN mapping table registers 9	$1C_H$	**53**
VLAN_Map_10	VLAN mapping table registers 10	$1D_H$	**53**

Table 9 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
VLAN_Map_11	VLAN mapping table registers 11	$1E_H$	53
VLAN_Map_12	VLAN mapping table registers 12	$1F_H$	53
VLAN_Map_13	VLAN mapping table registers 13	20_H	53
VLAN_Map_14	VLAN mapping table registers 14	21_H	53
VLAN_Map_15	VLAN mapping table registers 15	22_H	53
ResReg_7	Reserved Register 7	23_H	53
ResReg_8	Reserved Register 8	24_H	54
ResReg_9	Reserved Register 9	25_H	54
ResReg_10	Reserved Register 10	26_H	54
ResReg_11	Reserved Register 11	27_H	54
ConfigReg_4	Configuration Register 4	28_H	54
ConfigReg_5	Configuration Register 5	29_H	54
ConfigReg_6	Configuration Register 6	$2A_H$	55
ConfigReg_7	Configuration Register 7	$2B_H$	55
ConfigReg_8	Configuration Register	$2C_H$	56
ResReg_12	Reserved Register 12	$2D_H$	57
ResReg_13	Reserved Register 13	$2E_H$	57
PH_Restart	PHY Restart	$2F_H$	57
ConfigReg_	Miscellaneous Configuration Register 9	30_H	58
BWCon_0	Bandwidth Control Register 0	31_H	58
BWCon_1	Bandwidth Control Register 1	32_H	59
BWConEn	Bandwidth Control Enable Register	33_H	60

The register is addressed wordwise.

Table 10 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)

Table 10 Register Access Types (cont'd)

Mode	Symbol	Description HW	Description SW
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is read and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW.

Table 11 Registers Clock Domains

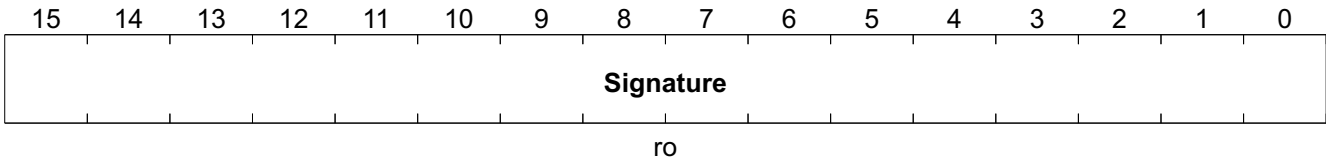
Clock Short Name	Description
–	–

4.1.1 EEPROM Contents

Signature Register

Description

SigReg	Offset	Reset Value
Signature Register	**00_H**	**4154_H**



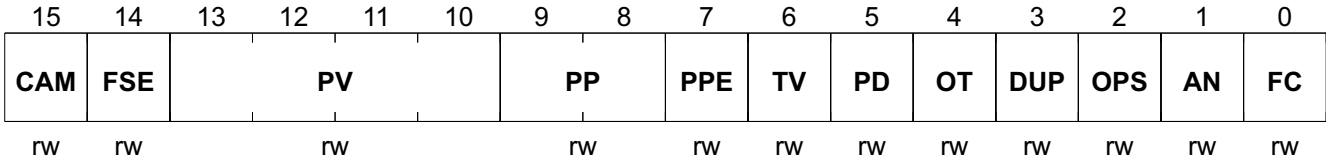
Field	Bits	Type	Description
Signature	15:0	ro	**Signature** 4154_H **SigReg**, Obligatory value (AT)

Note: ADM6996F will check register 0 value before reading all EEPROM content. If this value does not match with 0x4154h then other values in EEPROM will be useless. ADM6996F will use internal default value. Users cannot write to Signature register when programming ADM6996F internal registers.

Basic Control Register 0

Used to configure chip settings

CtrlReg_0	Offset	Reset Value
Basic Control Register 0	**01_H**	**$040F_H$**



15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAM	**FSE**	**PV**				**PP**		**PPE**	**TV**	**PD**	**OT**	**DUP**	**OPS**	**AN**	**FC**
rw	rw	rw				rw		rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CAM	15	rw	**Crossover Auto MDIX** 0_B **D**, Disable *Note: Hardware Reset latch value EECK can be set globally using the Auto MDIX function.* 1_B **E**, Enable
FSE	14	rw	**Fx Select Enable** 0_B **TP**, Tp Mode *Note: If this bit has been set to Fx in hardware then the bit does not have the power to change from Fx to Tp* 1_B **FX**, Fx Mode
PV	13 :10	rw	**Port VLAN ID**
PP	9:8	rw	**Port Based Priority**
PPE	7	rw	**Port Based Priority Enable** 0_B **VTE**, VLAN or TOS Priority Enable *Note: This bit is default 0_B to enable VLAN or TOS priority check. If users would like to check the VLAN priority, Tag mode should be enabled.* 1_B **PBE**, Port Based Priority Enable *Note: If this bit set to 1_B, only port based priority will be checked.*
TV	6	rw	**TOS over VLAN priority** 0_B **V**, VLAN Enable 1_B **T**, TOS Enable
PD	5	rw	**Port Disable** 0_B **E**, Enable 1_B **D**, Disable
OT	4	rw	**Output Packet Tagging** 0_B **U**, Un-tag 1_B **T**, Tag

Field	Bits	Type	Description
DUP	3	rw	**Duplex Enable** 0_B **H**, Half 1_B **F**, Full
OPS	2	rw	**Operating Speed** 0_B **10**, 10 Mbit/s 1_B **100**, 100 Mbit/s
AN	1	rw	**Auto-negotiation** 0_B **D**, Disable 1_B **E**, Enable
FC	0	rw	**802.x Flow Control Command** 0_B **D**, Disable 1_B **E**, Enable

Similar Registers

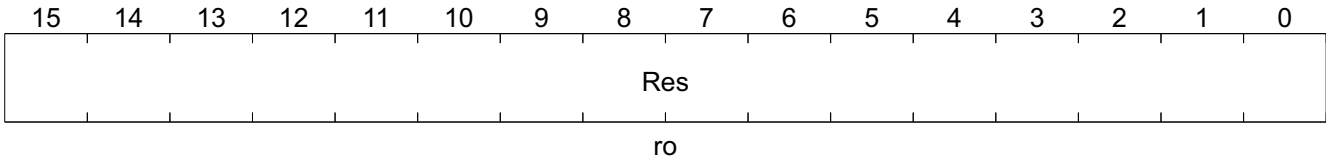
Table 12 Basic Control Registers 1 to 4

Register Short Name	Register Long Name	Offset Address	Page Number
CtrlReg_P1	Basic Control Register 1	03_H	
CtrlReg_P2	Basic Control Register 2	05_H	
CtrlReg_P3	Basic Control Register 3	07_H	
CtrlReg_P4	Basic Control Register 4	08_H	

Reserved Register 0

Register reserved for future use

ResReg_0	Offset	Reset Value
Reserved Register 0	**02_H**	**$040F_H$**



Field	Bits	Type	Description
Res	15:0	ro	**Reserved**

Similar Registers

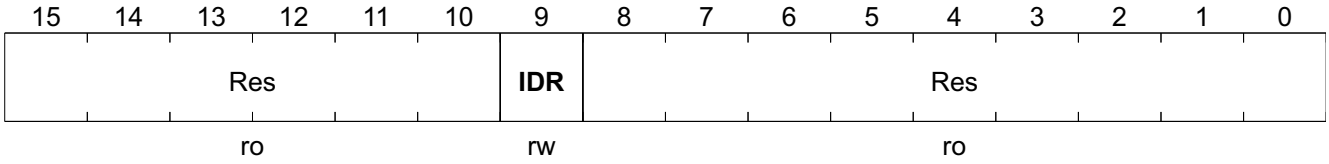
Table 13 Reserved Register 1 to 3

Register Short Name	Register Long Name	Offset Address	Page Number
ResReg_1	Reserved Register 1	04_H	
ResReg_2	Reserved Register 2	06_H	
ResReg_3	Reserved Register 3	09_H	

Reserved Register 4

Register reserved for future use

ResReg_4	Offset	Reset Value
Reserved Register 4	**$0A_H$**	**5902_H**

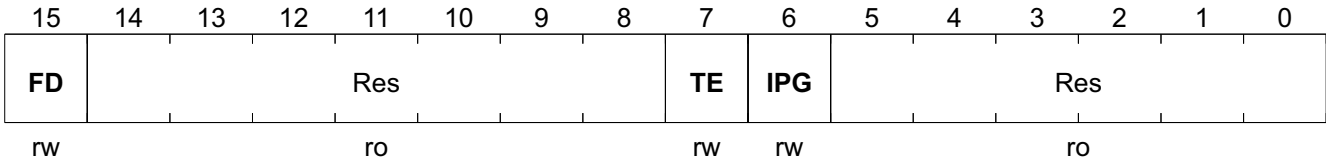


Field	Bits	Type	Description
Res	15:10	ro	**Reserved**
IDR	9	rw	**Replace Packet ID** 0_B , Not replaced 1_B , Replaced with VID 0&1 by PVID
Res	8:0	ro	**Reserved**

Configuration Register 1

Used to configure the chip

ConfigReg_1	Offset	Reset Value
Configuration Register 1	**$0B_H$**	**8000_H**



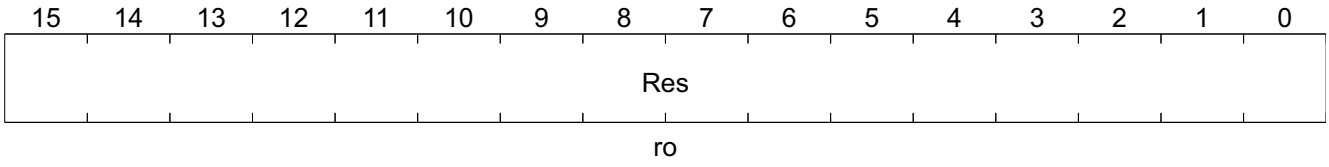
Field	Bits	Type	Description
FD	15	rw	**Far End Fault Detection** 0_B **D**, Disable 1_B **E**, Enable
Res	14:8	ro	**Reserved**
TE	7	rw	**Trunk Enable** 0_B **D**, Disable Trunk of Port 3 and 4 1_B **E**, Enable Trunk of Port 3 and 4
IPG	6	rw	**Inter Packet Gap Setting** 0_B **96B**, 96 bits 1_B **92B**, 92 bits
Res	5:0	ro	**Reserved**

Reserved Register 5

Reserved for future use

ResReg_5 **Offset** **Reset Value**

Reserved Register 5 **$0C_H$** **$FA50_H$**



Field	Bits	Type	Description
Res	15:0	ro	**Reserved**

Similar Registers

Table 14 Reserved Register 6

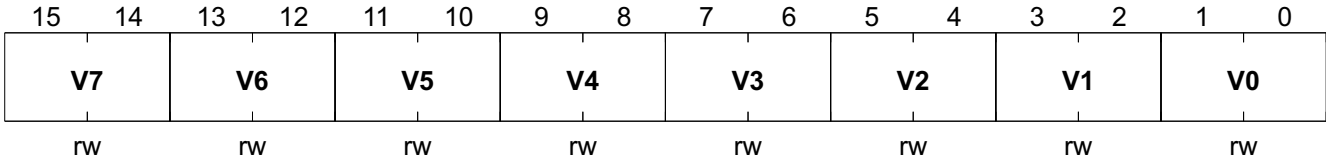
Register Short Name	Register Long Name	Offset Address	Page Number
ResReg_6	Reserved Register 6	$0D_H$	

VLAN Priority Map Register

Sets the VLAN priorities

VLAN_Map_P **Offset** **Reset Value**

VLAN priority Map Register **$0E_H$** **5500_H**



Field	Bits	Type	Description
V7	15:14	rw	**Mapped priority of tag value (VLAN)**
V6	13:12	rw	
V5	11:10	rw	
V4	9:8	rw	
V3	7:6	rw	
V2	5:4	rw	
V1	3:2	rw	
V0	1:0	rw	

Note: Value 3 ~ 0 are for priority queue Q3~Q0 respectively.The Weight ratio is Q3: Q2: Q1: Q0 = 8: 4: 2: 1. The default is port-base priority for un-tagged packets and non_IP frame.

Type of Service (TOS) Priority Map Register

Sets TOS priority

TOS_Priority	Offset	Reset Value
TOS priority Map Register	$0F_H$	5500_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T7		T6		T5		T4		T3		T2		T1		T0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
T7	15:14	rw	**Mapped priority of tag value (TOS)**
T6	13:12	rw	
T5	11:10	rw	
T4	9:8	rw	
T3	7:6	rw	
T2	5:4	rw	
T1	3:2	rw	
T0	1:0	rw	

Note: Value 3 ~ 0 are for priority queues Q3~Q0 respectively. The Weight ratio is Q3: Q2: Q1: Q0 = 8: 4: 2: 1. The default is port-based priority for un-tagged packets and non_IP frames.

Configuration Register 2

Used to configure the chip

ConfigReg_2	Offset	Reset Value
Configuration Register 2	10_H	0040_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Q3		Q2		Q1		Q0		AGE	Res	Res	XC	Res	SF	ST	
rw		rw		rw		rw		rw	ro	ro	rw	rw	rw	rw	

Field	Bits	Type	Description
Q3	15:14	rw	**Discard mode**
Q2	13:12	rw	Drop scheme for each Queue. See **Table 17** for details on the drop scheme of each queue
Q1	11:10	rw	
Q0	9:8	rw	

Field	Bits	Type	Description
AGE	7	rw	**Aging Status** 0_B **E**, Enable 1_B **D**, Disable
Res	6	ro	**Reserved**
Res	5	ro	**Reserved**
XC	4	rw	**CRC Check** 0_B **E**, Enable CRC check 1_B **D**, Disable CRC check
Res	3	rw	**Reserved**
SF	2	rw	**Broadcast Storm Filter** 0_B **D**, Disable 1_B **E**, Enable
ST	1:0	rw	**Broadcast Storm Threshold** See below **Table 15** and **Table 16** for details on the Broadcast Storm Threshold

Note: Broadcast storm initial time interval = 50ms. The max. packet number = 7490 in 100Base, 749 in 10Base

Table 15 Per Port Rising Threshold

	00	01	10	11
All 100TX	Disable	10%	20%	40%
Not All 100TX	Disable	1%	2%	4%

Table 16 Per Port Falling Threshold

	00	01	10	11
All 100TX	Disable	5%	10%	20%
Not All 100TX	Disable	0.5%	1%	2%

Table 17 Drop Scheme for Each Queue

Discard Mode Utilization	00	01	10	11
TBD	0%	0%	25%	50%

VLAN mode select Register

Selects VLAN Mode

VLAN_Mode	Offset	Reset Value
VLAN Mode Select Register	11_H	$FF00_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res								Res		**VM**	**MAC**	Res			
ro								ro		rw	rw	ro			

Field	Bits	Type	Description
Res	15:8	ro	**Reserved**
Res	7:6	ro	**Reserved**
VM	5	rw	**VLAN Mode Select** 0_B **P**, Port based by-pass mode 1_B **Q**, Tag based
MAC	4	rw	**MAC Clone Enable** 0_B **N**, Normal Mode. Learning with SA only. The MAC table will be searched or filled using only SA or DA. 1_B **M**, Mac Mode. Learned using SA VID0. MAC table will be searched or filled using VID0 SA or DA. This bit allows two identical addresses with different VID0 to be learned.
Res	3:0	ro	**Reserved**

Note:

Below is an example of a VLAN Tag and a MAC application for Bit4 and Bit5.

Below is an old router architecture example. The disadvantages of this are:

1. WAN port only supports 10M Half-Duplex and non-MDIX functions
2. Needs extra 10M NIC costs.
3. ISA bus will become a bottleneck for the whole system

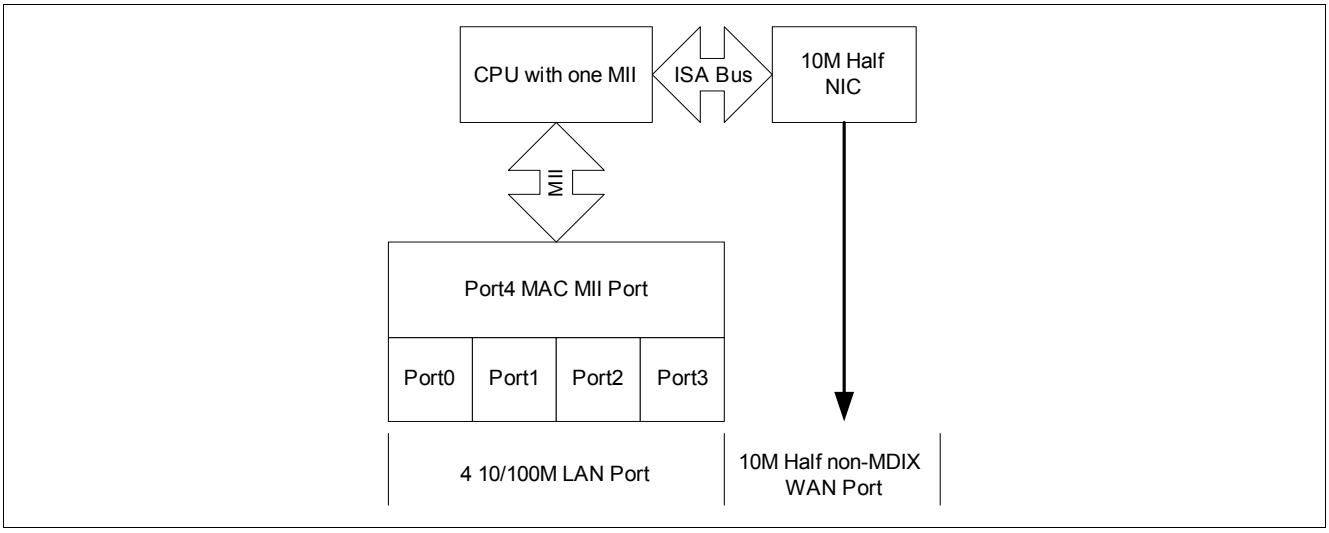


Figure 9 Old router architecture example

Below is new architecture by using ADM6996F serial chip VLAN function. The advantages of below are:

1. WAN Port can upgrade to 100/10 Full/Half, Auto MDIX.

2. WAN/LAN Port is programmable and put on same Switch.
3. No need extra NIC and save lot of costs.
4. High bandwidth of MII port up to 200M speed.

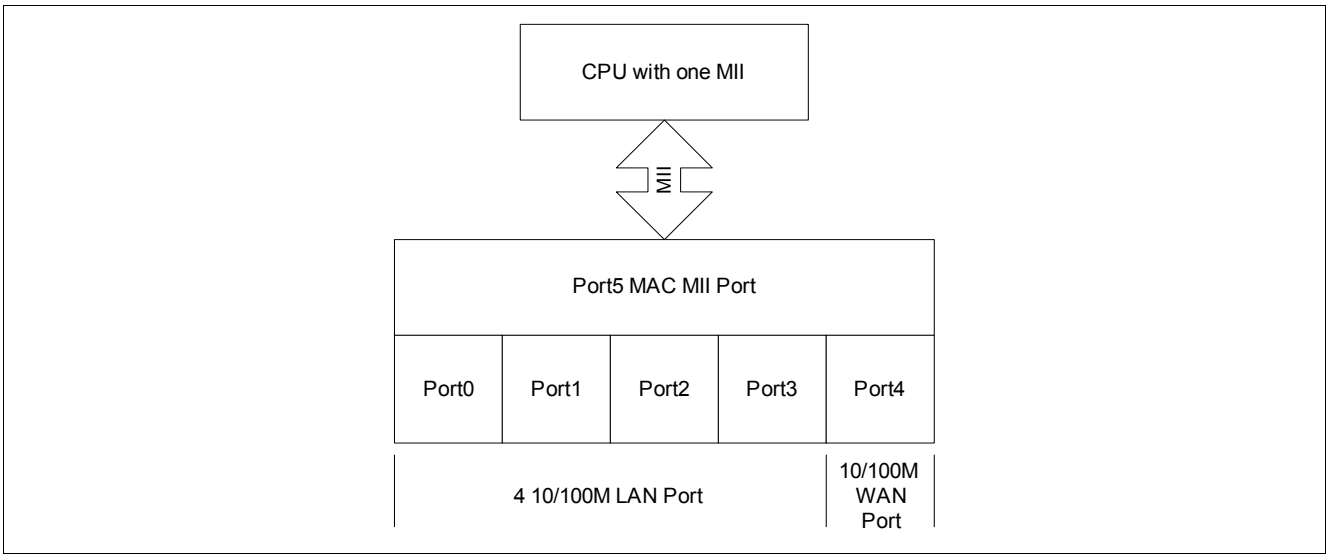


Figure 10 New Router Architecture Using ADM6996F

New Router applications work well on normal application. If user's ISP vendor(cable modem) lock Registration Card's ID then Router CPU must send this Lock Registration Card's ID to WAN Port. One condition which occurs is if there exists two of the same MAC IDs on this Switch: One is original Card and another one is CPU. This will cause Switch learning table problems.

ADM6996F provides a MAC Clone function that allows two same MAC addresses with different VLAN ID0 on a learning table. This will solve the Lock registration Card's ID issue. ADM6996F serial chip will put these two same MAC addresses with different VLAN ID0 at different learning table entry.

How to Set ADM6996F on Router

Port0~3: LAN Port.

Port4: WAN Port.

Port5: MII Port as CPU Port.

Step1: Set Register 0x11h bit4 and bit5 to 1.

{Coding: Write Register 0x11h as 0xff30h}

Step2: Set Port0~3 as Untag Port and set PVID=1.

{Coding: Write Register 0x01h, 0x03h, 0x05h, 0x07h as 0x840f. Port0~3 as Untag, PVID=1, Enable MDIX}

Step3: Set Port4 as Untag Port and set PVID=2.

{Coding:Write Register 0x08h as 0x880fh. Port4 as Untag, PVID=2, Enable MDIX.}

Step4: Set Port5 MII Port as Tag Port and set PVID=2.

{Coding:Write Register 0x09h as 0x881fh. Port5 MII port as Tag, PVID=2.}

Step5: Group Port0, 1, 2, 3, 5 as VLAN 1.

{Coding: Write Register 0x14h as 0x0155h. VLAN1 cover Port0, 1, 2, 3, 5.}

Step6: Group Port4, 5 as VLAN 2.

{Coding: Write Register 0x15h as 0x0180h. VLAN2 cover Port4, 5.}

How MAC Clone Operation

- LAN to LAN/CPU Traffic.

ADM6996F LAN traffic to LAN/CPU only. Traffic to another LAN port will be untag packet. Traffic to CPU is Tag packet with VID=1. CPU can check VID to distinguish LAN traffic or WAN traffic.

- WAN to CPU Traffic.

ADM6996F WAN traffic to CPU only. Traffic to CPU is Tag packet with VID=2. CPU can check VID to distinguish LAN traffic or WAN traffic.

- CPU to LAN Packet.

ADM6996F CPU Packet to LAN port must add VID=1 in VLAN field.
ADM6996F checks VID to distinguish LAN traffic or WAN traffic. LAN output packet is Untag.

- CPU to WAN Packet.

ADM6996F CPU Packet to WAN port must add VID=2 in VLAN filed.
ADM6996F checks VID to distinguish LAN traffic or WAN traffic. WAN output packet is Untag.

- ADM6996F learning sequence

ADM6996F will check VLAN map setting first then check learning table.
User doesn't need to worry LAN/WAN traffic mix up.
Bit 10: Half Duplex Back Pressure enable. 1/enable, 0/disable.

Configuration Register 3

ConfigReg_3	Offset	Reset Value
Miscellaneous Configuration Register 3	**12_H**	**3600_H**

15	14	13 12	11	10 9	8	7	6	5	4	3	2	1	0
CD	**DXCL**	Res	Res	Res	**ML5**	**ML4**	**ML3**	Res	**ML2**	Res	**ML1**	Res	**ML0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CD	15	rw	**Excessive Collision Drop** 0_B **D**, Disable 1_B **E**, Enable
DXCL	14	rw	**Duplex and Col Separate** 0_B **D**, Indicates the duplex and collision status at the same time 1_B **LM**, Indicates the duplex status only
Res	13:12	rw	**Reserved**
Res	11	rw	**Reserved**
Res	10:9	rw	**Reserved**
ML5	8	rw	**Port5 MAC Lock** 0_B **D**, Disable 1_B **LM**, Lock first MAC Source Address

Field	Bits	Type	Description
ML4	7	rw	**Port4 MAC Lock** 0_B **D**, Disable 1_B **LM**, Lock first MAC Source Address
ML3	6	rw	**Port3 MAC Lock** 0_B **D**, Disable 1_B **LM**, Lock first MAC Source Address
Res	5	rw	**Reserved**
ML2	4	rw	**Port 2 MAC Lock** 0_B **D**, Disable 1_B **LM**, Lock first MAC source address
Res	3	rw	**Reserved**
ML1	2	rw	**Port1 MAC Lock** 0_B **D**, Disable 1_B **LM**, Lock first MAC source address
Res	1	rw	**Reserved**
ML0	0	rw	**Port0 MAC Lock** 0_B **D**, Disable 1_B **LM**, Lock first MAC source address

VLAN Mapping Table Registers 0

VLAN_Map_0	Offset	Reset Value
VLAN mapping table registers 0	13_H	$FFFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res							**VM5**	**VM4**	**VM3**	Res	**VM2**	Res	**VM1**	Res	**VM0**
ro							rw	rw	rw	ro	rw	ro	rw	ro	rw

Field	Bits	Type	Description
Res	15:9	ro	**Reserved**
VM5	8	rw	**Port 5 VLAN Mapping** 0_B **NM**, Port 5 is not the member of the VLAN. 1_B **M**, Port 5 is the member of the VLAN.
VM4	7	rw	**Port 4 VLAN Mapping** 0_B **NM**, Port 4 is not the member of the VLAN. 1_B **M**, Port 4 is the member of the VLAN.
VM3	6	rw	**Port 3 VLAN Mapping** 0_B **NM**, Port 3 is not the member of the VLAN. 1_B **M**, Port 3 is the member of the VLAN.
Res	5	ro	**Reserved**

Field	Bits	Type	Description
VM2	4	rw	**Port 2 VLAN Mapping** 0_B **NM**, Port 2 is not the member of the VLAN. 1_B **M**, Port 2 is the member of the VLAN.
Res	3	ro	**Reserved**
VM1	2	rw	**Port 1 VLAN Mapping** 0_B **NM**, Port 1 is not the member of the VLAN. 1_B **M**, Port 1 is the member of the VLAN.
Res	1	ro	**Reserved**
VM0	0	rw	**Port 0 VLAN Mapping** 0_B **NM**, Port 0 is not the member of the VLAN. 1_B **M**, Port 0 is the member of the VLAN.

Note: 16 VLAN Group: See Register 0x2ch bit 11. Select the VLAN group ports and set the corresponding bits to 1.

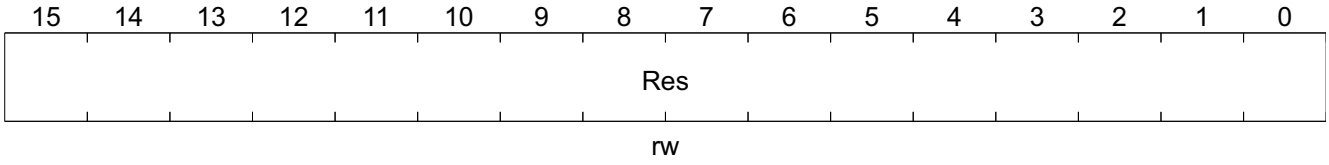
Similar Registers

Table 18 Basic Control Registers 1 to 4

Register Short Name	Register Long Name	Offset Address	Page Number
VLAN_Map_1	VLAN mapping table registers 1	14_H	
VLAN_Map_2	VLAN mapping table registers 2	15_H	
VLAN_Map_3	VLAN mapping table registers 3	16_H	
VLAN_Map_4	VLAN mapping table registers 4	17_H	
VLAN_Map_5	VLAN mapping table registers 5	18_H	
VLAN_Map_6	VLAN mapping table registers 6	19_H	
VLAN_Map_7	VLAN mapping table registers 7	$1A_H$	
VLAN_Map_8	VLAN mapping table registers 8	$1B_H$	
VLAN_Map_9	VLAN mapping table registers 9	$1C_H$	
VLAN_Map_10	VLAN mapping table registers 10	$1D_H$	
VLAN_Map_11	VLAN mapping table registers 11	$1E_H$	
VLAN_Map_12	VLAN mapping table registers 12	$1F_H$	
VLAN_Map_13	VLAN mapping table registers 13	20_H	
VLAN_Map_14	VLAN mapping table registers 14	21_H	
VLAN_Map_15	VLAN mapping table registers 15	22_H	

Reserved Register 7

ResReg_7	Offset	Reset Value
Reserved Register 7	**23_H**	**0000_H**



Field	Bits	Type	Description
Res	15:0	rw	**Reserved**

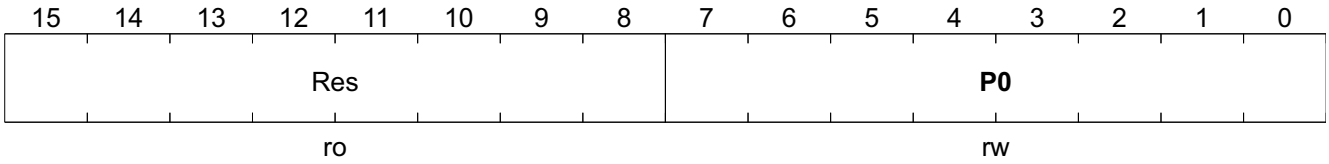
Similar Registers

Table 19 Reserved Register 8 to 11

Register Short Name	Register Long Name	Offset Address	Page Number
ResReg_8	Reserved Register 8	24_H	
ResReg_9	Reserved Register 9	25_H	
ResReg_10	Reserved Register 10	26_H	
ResReg_11	Reserved Register 11	27_H	

Configuration Register 4

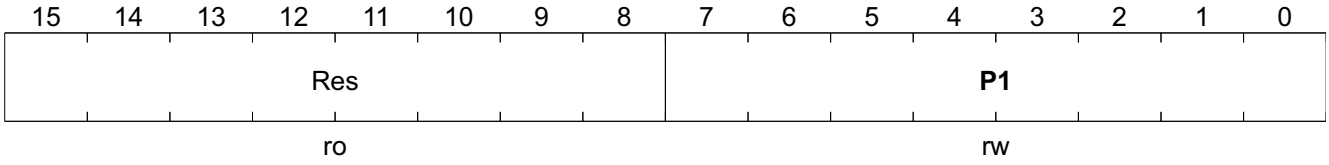
ConfigReg_4	Offset	Reset Value
Configuration Register 4	**28_H**	**0000_H**



Field	Bits	Type	Description
Res	15:8	ro	**Reserved**
P0	7:0	rw	**Port 0 PVID** 0001_H **PVID**, These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.

Configuration Register 5

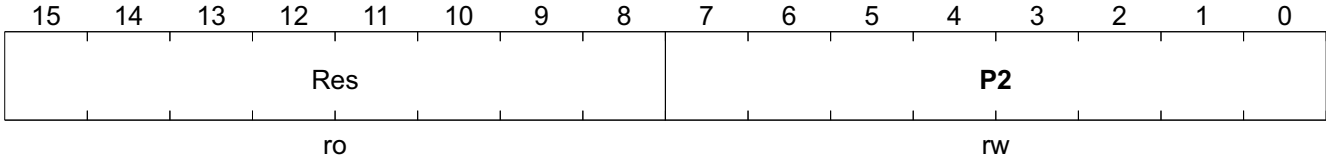
ConfigReg_5	Offset	Reset Value
Configuration Register 5	**29_H**	**0000_H**



Field	Bits	Type	Description
Res	15:8	ro	**Reserved**
P1	7:0	rw	**Port1 PVID bit 11~4.** 0003_H **PVID 1**, These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.

Configuration Register 6

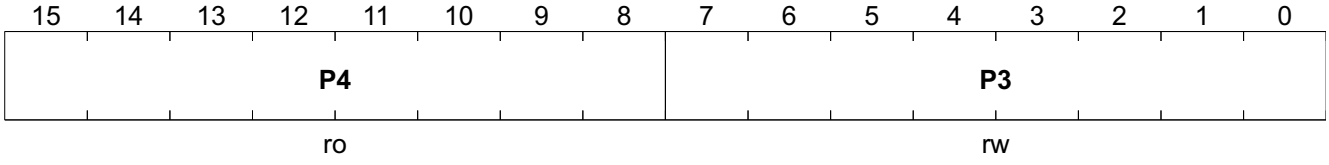
ConfigReg_6	Offset	Reset Value
Configuration Register 6	**$2A_H$**	**0000_H**



Field	Bits	Type	Description
Res	15:8	ro	**Reserved**
P2	7:0	rw	**Port2 PVID bit 11~4.** 0005_H **PVID 2**, These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.

Configuration Register 7

ConfigReg_7	Offset	Reset Value
Configuration Register 7	**$2B_H$**	**0000_H**



Field	Bits	Type	Description
P4	15:8	ro	**Port4 PVID bit 11~4.** 0008_H **PVID 1**, These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.

Field	Bits	Type	Description
P3	7:0	rw	**Port3 PVID bit 11~4.** 0007_H **PVID 1**, These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.

Configuration Register 8

ConfigReg_8	Offset	Reset Value
Configuration Register	$2C_H$	$D000_H$

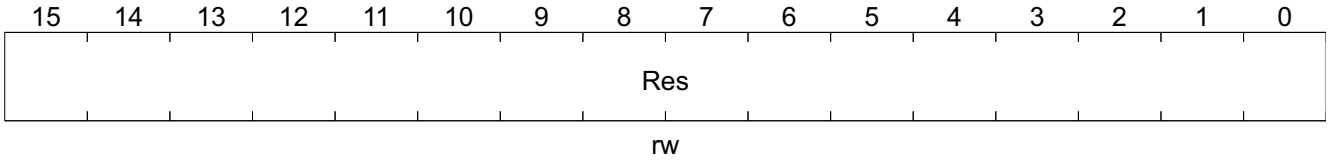
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR0	**CR1**	**CR2**	**CR3**	Res	**VS**			**P5**							
rw	rw	rw	rw	rw	rw			rw							

Field	Bits	Type	Description
CR0	15	rw	**Control Reserved MAC** Control reserved MAC (0180C2000000) 0_B **D**, Discard 1_B **F**, Forward
CR1	14	rw	**Control Reserved MAC** Control reserved MAC (0180C2000001) 0_B **D**, Discard 1_B **F**, Forward
CR2	13	rw	**Control Reserved MAC** Control reserved MAC (0180C2000002- 0180C200000F) 0_B **D**, Discard 1_B **F**, Forward
CR3	12	rw	**Control Reserved MAC** Control reserved MAC (0180C2000010-0180C20000FF) 0_B **D**, Discard 1_B **F**, Forward
Res	11	rw	**Reserved**
VS	10:8	rw	**VLAN Grouping Tag Shift** 0_D **VID0**, VID [3:0] 1_D **VID1**, VID [4:1] 2_D **VID2**, VID [5:2] 3_D **VID3**, VID [6:3] 4_D **VID4**, VID [7:4] 5_D **VID5**, VID [8:5] 6_D **VID6**, VID [9:6] 7_D **VID7**, VID [10:7]
P5	7:0	rw	**Port5 PVID bit 11~4.** 0009_H **PVID 1**, These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.

Note: Bit[10:8]: VLAN Tag shift register. ADM6996F will select 4 bit form total 12 bit VID as VLAN group reference. Bit[15:12]: IEEE 802.3 reserved DA forward or drop police.

Reserved Register 12

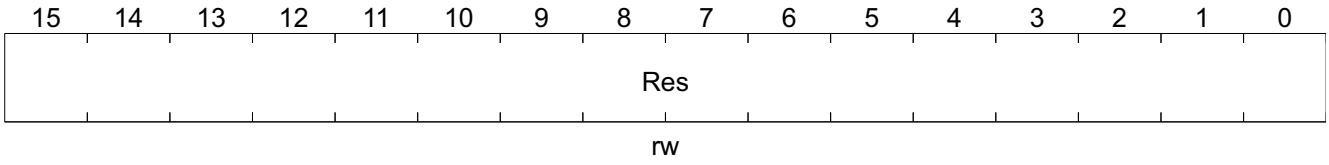
ResReg_12	Offset	Reset Value
Reserved Register 12	**$2D_H$**	**4442_H**



Field	Bits	Type	Description
Res	15:0	rw	**Reserved**

Reserved Register 13

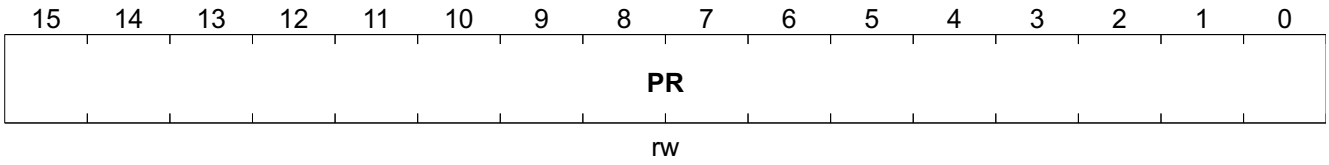
ResReg_13	Offset	Reset Value
Reserved Register 13	**$2E_H$**	**0000_H**



Field	Bits	Type	Description
Res	15:0	rw	**Reserved**

PHY Restart

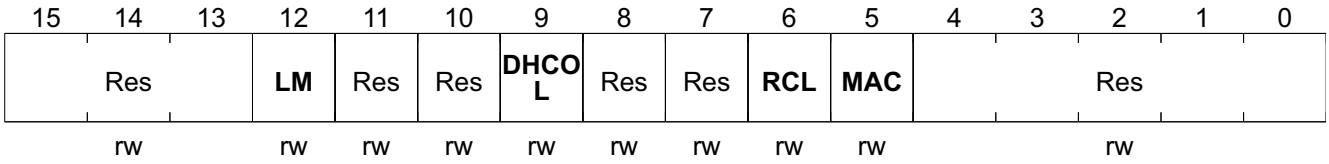
PH_Restart	Offset	Reset Value
PHY Restart	**$2F_H$**	**0000_H**



Field	Bits	Type	Description
PR	15:0	rw	**PHY Restart** 0000_H **PHY Restart**, Writing this Hex value to this register restarts the internal PHYs.

Configuration Register 9

ConfigReg_	Offset	Reset Value
Miscellaneous Configuration Register 9	**30_H**	**0987_H**



Field	Bits	Type	Description
Res	15:13	rw	**Reserved**
LM	12	rw	**Port 4 LED Mode** 0_B **D**, LinkAct/DupCol/Speed 1_B **S**, LinkAct/Speed
Res	11	rw	**Reserved**
Res	10	rw	**Reserved**
DHCOL	9	rw	**Dual Speed Hub COL_LED Enable** 0_B **N**, Normal LED display. 1_B **D**, Dual Speed Hub LED display. Port0 Col LED: 10M Col LED. Port1 Col LED: 100M Col LED.
Res	8	rw	**Reserved**
Res	7	rw	**Reserved**
RCL	6	rw	**MII Speed Double** 0_B **25**, TxCLK max speed is 25 MHz 1_B **50**, TxCLK max speed is 50 MHz
MAC	5	rw	**Mac Clone Enable** MAC Clone Enable Bit[1].
Res	4:0	rw	**Reserved**

Bandwidth Control Register

BWCon_0	Offset	Reset Value
Bandwidth Control Register 0	**31_H**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RC3	**P3T**			**RC2**	**P2T**			**RC1**	**P1T**			**RC0**	**P0T**		
rw	rw			rw	rw			rw	rw			rw	rw		

Field	Bits	Type	Description
RC3	15	rw	**Receive Packet Length Count** Counted on the Source Port 3. 0_D **R3**, The switch will add length to the P3 counter
P3T	14:12	rw	**Port 3 Threshold Control Meter** Reference **Table 20** in note below.
RC2	11	rw	**Receive Packet Length Count** Counted on the Source Port 2. 0_D **R2**, The switch will add length to the P2 counter
P2T	10:8	rw	**Port 2 Threshold Control Meter** Reference **Table 20** in note below.
RC1	7	rw	**Receive Packet Length Count** Counted on the Source Port 1. 0_D **R1**, The switch will add length to the P1 counter
P1T	6:4	rw	**Port 1 Threshold Control Meter** Reference **Table 20** in note below.
RC0	3	rw	**Receive Packet Length Count** Counted on the Source Port 0. 0_D **R0**, The switch will add length to the P2 counter
P0T	2:0	rw	**Port 0 Threshold Control Meter** Reference **Table 20** in note below.

Table 20 Note:Reference Table

000	001	010	011	100	101	110	111
256K	512K	1M	2M	5M	10M	20M	50M

Bandwidth Control Register 1

BWCon_1 **Offset** **Reset Value**

Bandwidth Control Register 1 **32_H** **0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res								**RC5**	**P5T**			**RC4**	**P4T**		
ro								rw	rw			rw	rw		

Field	Bits	Type	Description
Res	15:8	ro	**Reserved**
RC5	7	rw	**Receive Packet Length Count** Counted on the Source Port 5. 0_D **Count5**, The switch will add length to the P5 counter
P5T	6:4	rw	**Port 5 Threshold Control Meter** Reference **Table 20** in note below.
RC4	3	rw	**Receive Packet Length Count** Counted on the Source Port 4. 0_D **Count4**, The switch will add length to the P4 counter
P4T	2:0	rw	**Port 4 Threshold Control Meter** Reference **Table 20** in note below.

Bandwidth Control Enable Register

BWConEn	Offset	Reset Value
Bandwidth Control Enable Register	**33_H**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res							**BW5**	**BW4**	**BW3**	Res	**BW2**	Res	**BW1**	Res	**BW0**
ro							rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Res	15:9	ro	**Reserved**
BW5	8	rw	**Port 5 Bandwidth Control Enable** 0_B **D**, Disable 1_B **E**, Enable
BW4	7	rw	**Port 4 Bandwidth Control Enable** 0_B **D**, Disable 1_B **E**, Enable
BW3	6	rw	**Port 3 Bandwidth Control Enable** 0_B **D**, Disable 1_B **E**, Enable
Res	5	rw	**Reserved**
BW2	4	rw	**Port 2 Bandwidth Control Enable** 0_B **D**, Disable 1_B **E**, Enable
Res	3	rw	**Reserved**
BW1	2	rw	**Port 1 Bandwidth Control Enable** 0_B **D**, Disable 1_B **E**, Enable
Res	1	rw	**Reserved**

Field	Bits	Type	Description
BW0	0	rw	**Port 0 Bandwidth Control Enable** 0_B **D**, Disable 1_B **E**, Enable

4.2 Serial Register Map

Table 21 Registers Address Space

Module	Base Address	End Address	Note
Serial Registers	00_H	$3C_H$	Independent Address Space

Table 22 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
ChipID	Chip Identifier Register	00_H	64
PortStat_0	Port Status Register 0	01_H	64
PortStat_1	Port Status Register 1	02_H	66
CabStat	Cable Broken Status	03_H	67
P0_RP_CNT	Port 0 Receive Packet Count	04_H	68
P1_RP_CNT	Port 1 Receive Packet Count	06_H	68
P2_RP_CNT	Port 2 Receive Packet Count	08_H	68
P3_RP_CNT	Port 3 Receive Packet Count	$0A_H$	68
P4_RP_CNT	Port 4 Receive Packet Count	$0B_H$	68
P5_RP_CNT	Port 5 Receive Packet Count	$0C_H$	68
P0_RB_CNT	Port 0 Receive Byte Count	$0D_H$	68
P1_RB_CNT	Port 1 Receive Byte Count	$0F_H$	68
P2_RB_CNT	Port 2 Receive Byte Count	11_H	68
P3_RB_CNT	Port 3 Receive Byte Count	13_H	68
P4_RB_CNT	Port 4 Receive Byte Count	14_H	68
P5_RB_CNT	Port 5 Receive Byte Count	15_H	68
P0_TP_CNT	Port 0 Transmit Packet Count	16_H	68
P1_TP_CNT	Port 1 Transmit Packet Count	18_H	68
P2_TP_CNT	Port 2 Transmit Packet Count	$1A_H$	68
P3_TP_CNT	Port 3 Transmit Packet Count	$1C_H$	68
P4_TP_CNT	Port 4 Transmit Packet Count	$1D_H$	68
P5_TP_CNT	Port 5 Transmit Packet Count	$1E_H$	68
P0_TB_CNT	Port 0 Transmit Byte Count	$1F_H$	68
P1_TB_CNT	Port 1 Transmit Byte Count	21_H	68
P2_TB_CNT	Port 2 Transmit Byte Count	23_H	68
P3_TB_CNT	Port 3 Transmit Byte Count	25_H	68
P4_TB_CNT	Port 4 Transmit Byte Count	26_H	68
P5_TB_CNT	Port 5 Transmit Byte Count	27_H	68
P0_COL_CNT	Port 0 Collision Count	28_H	68
P1_COL_CNT	Port 1 Collision Count	$2A_H$	68
P2_COL_CNT	Port 2 Collision Count	$2C_H$	69
P3_COL_CNT	Port 3 Collision Count	$2E_H$	69
P4_COL_CNT	Port 4 Collision Count	$2F_H$	69
P5_COL_CNT	Port 5 Collision Count	30_H	69

Table 22 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
P0_ERR_CNT	Port 0 Error Count	31_H	69
P1_ERR_CNT	Port 1 Error Count	33_H	69
P2_ERR_CNT	Port 2 Error Count	35_H	69
P3_ERR_CNT	Port 3 Error Count	37_H	69
P4_ERR_CNT	Port 4 Error Count	38_H	69
P5_ERR_CNT	Port 5 Error Count	39_H	69
OverFlow_0	Over Flow Flag Register 0	$3A_H$	69
OverFlow_1	Over Flow Flag Register 1	$3B_H$	70
OverFlow_2	Over Flow Flag Register 2	$3C_H$	70

The register is addressed wordwise.

Table 23 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register

Table 23 Register Access Types (cont'd)

Mode	Symbol	Description HW	Description SW
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is read and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW.

Table 24 Registers Clock Domains

Clock Short Name	Description
–	–

4.2.1 Serial Registers

Chip Identifier Register

ChipID	Offset	Reset Value
Chip Identifier Register	00_H	$0007\ 1010_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																												Ver			
ro																												ro			

Field	Bits	Type	Description
ID	31:4	ro	**Chip Identifier Register** $000\ 7101_H$ **ID**, Chip Identifier
Ver	3:0	ro	**Version No** 2_H **Ver**, Version No.

Port Status Register 0

PortStat_0	Offset	Reset Value
Port Status Register 0	01_H	$0000\ 0000_H$

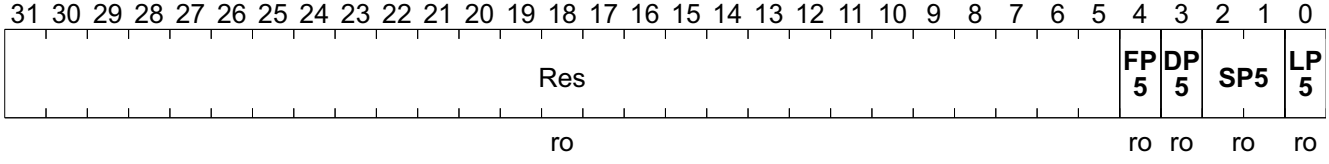
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FP4	DP4	SP4	LP4	FP3	DP3	SP3	LP3	Res	Res	Res	Res	FP2	DP2	SP2	LP2	Res	Res	Res	Res	FP1	DP1	SP1	LP1	Res	Res	Res	Res	FP0	DP0	SP0	LP0
ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
FP4	31	ro	**Port 4 Flow Control Enable** 0_B **D**, Flow Control Disable 1_B **FC4**, 802.3X on for full duplex or back pressure on for half duplex.
DP4	30	ro	**Port 4 Duplex Status** 0_B **H**, Half Duplex 1_B **F**, Full Duplex
SP4	29	ro	**Port 4 Speed Status** 0_B **10**, 10 Mbit/s 1_B **100**, 100 Mbit/s
LP4	28	ro	**Port 4 Linkup Status** 0_B **NE**, Link is not established. 1_B **E**, Link is established.
FP3	27	ro	**Port 3 Flow Control Enable** 0_B **D**, Flow Control Disable 1_B **FC3**, 802.3X on for full duplex or back pressure on for half duplex.
DP3	26	ro	**Port 3 Duplex Status** 0_B **H**, Half Duplex 1_B **F**, Full Duplex
SP3	25	ro	**Port 3 Speed Status** 0_B **10**, 10 Mbit/s 1_B **100**, 100 Mbit/s
LP3	24	ro	**Port 3 Linkup Status** Port 3 Linkup Status: 0_B **N**, Link is not established. 1_B **E**, Link is established.
Res	23	ro	**Reserved**
Res	22	ro	**Reserved**
Res	21	ro	**Reserved**
Res	20	ro	**Reserved**
FP2	19	ro	**Port 2 Flow Control Enable** 0_B **D**, Flow Control Disable 1_B **FC2**, 802.3X on for full duplex or back pressure on for half duplex.
DP2	18	ro	**Port 2 Duplex Status** 0_B **H**, Half Duplex 1_B **F**, Full Duplex
SP2	17	ro	**Port 2 Speed Status** 0_B **10**, 10 Mbit/s 1_B **100**, 100 Mbit/s
LP2	16	ro	**Port 2 Linkup Status** Port 2 Linkup Status: 0_B **NE**, Link is not established. 1_B **E**, Link is established.
Res	15	ro	**Reserved**
Res	14	ro	**Reserved**
Res	13	ro	**Reserved**

Field	Bits	Type	Description
Res	12	ro	**Reserved**
FP1	11	ro	**Port 1 Flow Control Enable** 0_B **D**, Flow Control Disable 1_B **FC1**, 802.3X on for full duplex or back pressure on for half duplex.
DP1	10	ro	**Port 1 Duplex Status** 0_B **H**, Half Duplex 1_B **F**, Full Duplex
SP1	9	ro	**Port 1 Speed Status** 0_B **10**, 10 Mbit/s 1_B **100**, 100 Mbit/s
LP1	8	ro	**Port 1 Linkup Status** 0_B **NE**, Not established. 1_B **E**, Established.
Res	7	ro	**Reserved**
Res	6	ro	**Reserved**
Res	5	ro	**Reserved**
Res	4	ro	**Reserved**
FP0	3	ro	**Port 0 Flow Control Enable** 0_B **D**, Flow Control Disable 1_B **FC0**, 802.3X on for full duplex or back pressure on for half duplex.
DP0	2	ro	**Port 0 Duplex Status** 0_B **H**, Half Duplex 1_B **F**, Full Duplex
SP0	1	ro	**Port 0 Speed Status** 0_B **10**, 10 Mbit/s 1_B **100**, 100 Mbit/s
LP0	0	ro	**Port 0 Linkup Status** 0_B **NE**, Not established. 1_B **E**, Established.

Port Status Register 1

PortStat_1	Offset	Reset Value
Port Status Register 1	**02_H**	**$0000\ 0000_H$**

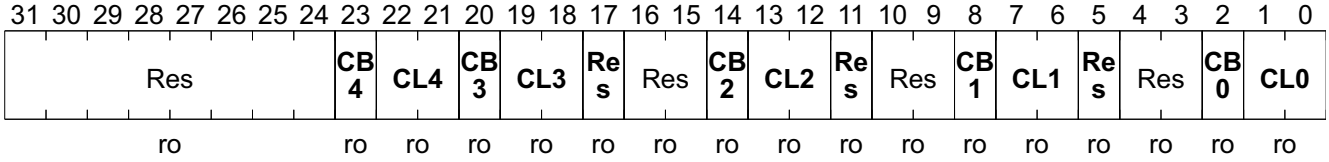


Field	Bits	Type	Description
Res	31:5	ro	**Reserved**

Field	Bits	Type	Description
FP5	4	ro	**Port 5 Flow Control Enable** 0_B **D**, Flow Control Disable 1_B **FC5**, 802.3X on for full duplex or back pressure on for half duplex.
DP5	3	ro	**Port 5 Duplex Status** 0_B **H**, Half Duplex 1_B **F**, Full Duplex
SP5	2:1	ro	**Port 5 Speed Status** 0_B **10**, 10 Mbit/s 1_B **100**, 100 Mbit/s
LP5	0	ro	**Port 5 Linkup Status** 0_B **NE**, Not established. 1_B **E**, Established.

Cable Broken Status Register

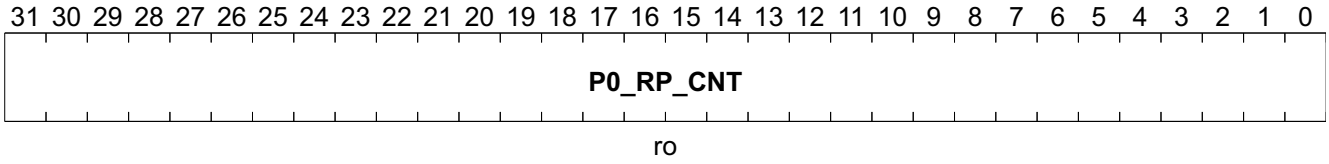
CabStat	Offset	Reset Value
Cable Broken Status	**03_H**	**$0000\ 0000_H$**



Field	Bits	Type	Description
Res	31:24	ro	**Reserved**
CB4	23	ro	**Port 4 Cable Broken**
CL4	22:21	ro	**Port 4 Cable Broken Length**
CB3	20	ro	**Port 3 Cable Broken**
CL3	19:18	ro	**Port 3 Cable Broken Length**
Res	17	ro	**Reserved**
Res	16:15	ro	**Reserved**
CB2	14	ro	**Port 2 Cable Broken**
CL2	13:12	ro	**Port 2 Cable Broken Length**
Res	11	ro	**Reserved**
Res	10:9	ro	**Reserved**
CB1	8	ro	**Port 1 Cable Broken**
CL1	7:6	ro	**Port 1 Cable Broken Length**
Res	5	ro	**Reserved**
Res	4:3	ro	**Reserved**
CB0	2	ro	**Port 0 Cable Broken**
CL0	1:0	ro	**Port 0 Cable Broken Length**

Port 0 Receive Packet Count

P0_RP_CNT	Offset	Reset Value
Port 0 Receive Packet Count	04_H	$0000\ 0000_H$



Field	Bits	Type	Description
P0_RP_CNT	31:0	ro	**Counter**

Similar Registers

Table 25 Per Port Counters

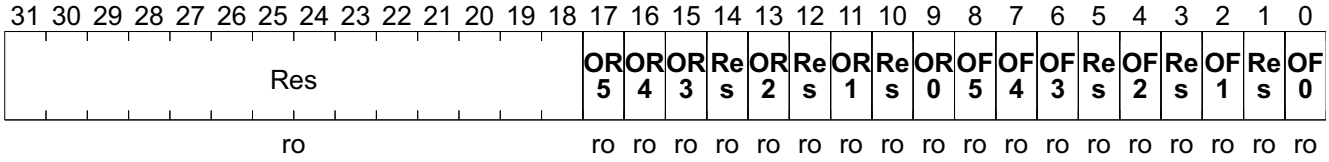
Register Short Name	Register Long Name	Offset Address	Page Number
P1_RP_CNT	Port 1 Receive Packet Count	06_H	
P2_RP_CNT	Port 2 Receive Packet Count	08_H	
P3_RP_CNT	Port 3 Receive Packet Count	$0A_H$	
P4_RP_CNT	Port 4 Receive Packet Count	$0B_H$	
P5_RP_CNT	Port 5 Receive Packet Count	$0C_H$	
P0_RB_CNT	Port 0 Receive Byte Count	$0D_H$	
P1_RB_CNT	Port 1 Receive Byte Count	$0F_H$	
P2_RB_CNT	Port 2 Receive Byte Count	11_H	
P3_RB_CNT	Port 3 Receive Byte Count	13_H	
P4_RB_CNT	Port 4 Receive Byte Count	14_H	
P5_RB_CNT	Port 5 Receive Byte Count	15_H	
P0_TP_CNT	Port 0 Transmit Packet Count	16_H	
P1_TP_CNT	Port 1 Transmit Packet Count	18_H	
P2_TP_CNT	Port 2 Transmit Packet Count	$1A_H$	
P3_TP_CNT	Port 3 Transmit Packet Count	$1C_H$	
P4_TP_CNT	Port 4 Transmit Packet Count	$1D_H$	
P5_TP_CNT	Port 5 Transmit Packet Count	$1E_H$	
P0_TB_CNT	Port 0 Transmit Byte Count	$1F_H$	
P1_TB_CNT	Port 1 Transmit Byte Count	21_H	
P2_TB_CNT	Port 2 Transmit Byte Count	23_H	
P3_TB_CNT	Port 3 Transmit Byte Count	25_H	
P4_TB_CNT	Port 4 Transmit Byte Count	26_H	
P5_TB_CNT	Port 5 Transmit Byte Count	27_H	
P0_COL_CNT	Port 0 Collision Count	28_H	
P1_COL_CNT	Port 1 Collision Count	$2A_H$	

Table 25 Per Port Counters

Register Short Name	Register Long Name	Offset Address	Page Number
P2_COL_CNT	Port 2 Collision Count	$2C_H$	
P3_COL_CNT	Port 3 Collision Count	$2E_H$	
P4_COL_CNT	Port 4 Collision Count	$2F_H$	
P5_COL_CNT	Port 5 Collision Count	30_H	
P0_ERR_CNT	Port 0 Error Count	31_H	
P1_ERR_CNT	Port 1 Error Count	33_H	
P2_ERR_CNT	Port 2 Error Count	35_H	
P3_ERR_CNT	Port 3 Error Count	37_H	
P4_ERR_CNT	Port 4 Error Count	38_H	
P5_ERR_CNT	Port 5 Error Count	39_H	

Over Flow Flag Register 0

OverFlow_0	Offset	Reset Value
Over Flow Flag Register 0	$3A_H$	$0000\ 0000_H$

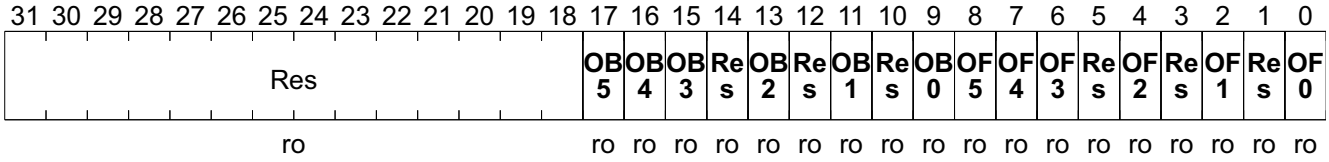


Field	Bits	Type	Description
Res	31:18	ro	**Reserved**
OR5	17	ro	**Overflow of Port 5 Receive Packet Byte Count**
OR4	16	ro	**Overflow of Port 4 Receive Packet Byte Count**
OR3	15	ro	**Overflow of Port 3 Receive Packet Byte Count**
Res	14	ro	**Reserved**
OR2	13	ro	**Overflow of Port 2 Receive Packet Byte Count**
Res	12	ro	**Reserved**
OR1	11	ro	**Overflow of Port 1 Receive Packet Byte Count**
Res	10	ro	**Reserved**
OR0	9	ro	**Overflow of Port 0 Receive Packet Byte Count**
OF5	8	ro	**Overflow of Port 5 Receive Packet Count**
OF4	7	ro	**Overflow of Port 4 Receive Packet Count**
OF3	6	ro	**Overflow of Port 3 Receive Packet Count**
Res	5	ro	**Reserved**
OF2	4	ro	**Overflow of Port 2 Receive Packet Count**
Res	3	ro	**Reserved**
OF1	2	ro	**Overflow of Port 1 Receive Packet Count**
Res	1	ro	**Reserved**

Field	Bits	Type	Description
OF0	0	ro	**Overflow of Port 0 Receive Packet Count**

Over Flow Flag Register 1

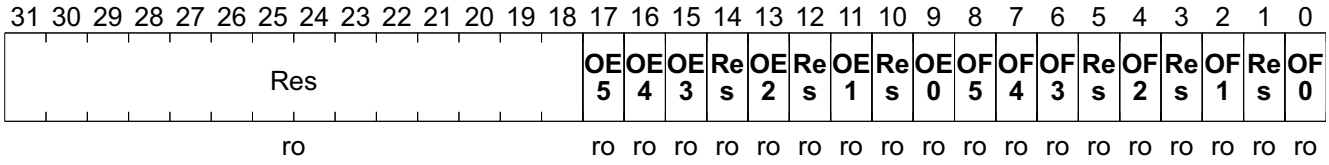
OverFlow_1	Offset	Reset Value
Over Flow Flag Register 1	**$3B_H$**	**0000 0000_H**



Field	Bits	Type	Description
Res	31:18	ro	**Reserved**
OB5	17	ro	**Overflow of Port 5 Transmit Packet Byte Count**
OB4	16	ro	**Overflow of Port 4 Transmit Packet Byte Count**
OB3	15	ro	**Overflow of Port 3 Transmit Packet Byte Count**
Res	14	ro	**Reserved**
OB2	13	ro	**Overflow of Port 2 Transmit Packet Byte Count**
Res	12	ro	**Reserved**
OB1	11	ro	**Overflow of Port 1 Transmit Packet Byte Count**
Res	10	ro	**Reserved**
OB0	9	ro	**Overflow of Port 0 Transmit Packet Byte Count**
OF5	8	ro	**Overflow of Port 5 Transmit Packet Count**
OF4	7	ro	**Overflow of Port 4 Transmit Packet Count**
OF3	6	ro	**Overflow of Port 3 Transmit Packet Count**
Res	5	ro	**Reserved**
OF2	4	ro	**Overflow of Port 2 Transmit Packet Count**
Res	3	ro	**Reserved**
OF1	2	ro	**Overflow of Port 1 Transmit Packet Count**
Res	1	ro	**Reserved**
OF0	0	ro	**Overflow of Port 0 Transmit Packet Count**

Over Flow Flag Register 2

OverFlow_2	Offset	Reset Value
Over Flow Flag Register 2	**$3C_H$**	**0000 0000_H**



Field	Bits	Type	Description
Res	31:18	ro	**Reserved**
OE5	17	ro	**Overflow of Port 5 Error Count**
OE4	16	ro	**Overflow of Port 4 Error Count**
OE3	15	ro	**Overflow of Port 3 Error Count**
Res	14	ro	**Reserved**
OE2	13	ro	**Overflow of Port 2 Error Count**
Res	12	ro	**Reserved**
OE1	11	ro	**Overflow of Port 1 Error Count**
Res	10	ro	**Reserved**
OE0	9	ro	**Overflow of Port 0 Error Count**
OF5	8	ro	**Overflow of Port 5 Collision Count**
OF4	7	ro	**Overflow of Port 4Collision Count**
OF3	6	ro	**Overflow of Port 3Collision Count**
Res	5	ro	**Reserved**
OF2	4	ro	**Overflow of Port 2 Collision Count**
Res	3	ro	**Reserved**
OF1	2	ro	**Overflow of Port 1 Collision Count**
Res	1	ro	**Reserved**
OF0	0	ro	**Overflow of Port 0 Collision Count**

4.3 Packet with Priority: Normal packet content

Table 26 Ethernet Packet from Layer 2

Preamble/SFD	Destination (6 bytes)	Source (6 bytes)	Packet length (2 bytes)	Data (46-1500 bytes)	CRC (4 bytes)
	Byte 0~5	Byte 6~11	Byte 12~13	Byte 14~	

4.4 VLAN Packet

Table 27 VLAN Packet

Tag Protocol TD 8100	Tag Control Information TCI	LEN Length	Routing Information
Byte 12~13	Byte14~15	Byte 16~17	Byte 18

Note: ADM6996F will check packet byte 12 &13. If byte[12:13]=8100h then this packet is a VLAN packet

Byte 14~15: Tag Control Information TCI

Bit[15:13]: User Priority 7~0

Bit 12: Canonical Format Indicator (CFI)

Bit[11~0]: VLAN ID. The ADM6996F will use bit[3:0] as VLAN group.

4.5 TOS IP Packet

Table 28 IP Packet

Type 0800	IP Header
Byte 12~13	Byte 14~15

Note: ADM6996F checks bytes 12 &13. If this value is 0800h then the ADM6996F knows this is a TOP priority packet.

IP header define

Byte 14

Bit[7:0]: IP protocol version number & header length.

Byte 15: Service type

Bit[7~5]: IP Priority (Precedence) from 7~0

Bit 4: No Delay (D)

Bit 3: High Throughput

Bit 2: High Reliability (R)

Bit[1:0]: Reserved

4.6 EEPROM Access

Users can select ADM6996F to read EEPROM contents as the chip setting or not. ADM6996F will check the signature of EEPROM, then decide to load contents of EEPROM or not.

Table 29 RESETL (RC) & EEPROM Content Relationship

RESETL	CS	SK	DI	DO
0	High Impedance	High Impedance	High Impedance	High Impedance
Rising edge 01 (30ms)	Output	Output	Output	Input
1 (after 30ms)	Input	Input	Output	Input

Keep at least 30ms after RESETL from 01. ADM6996F will read data from EEPROM. After RESETL if CPU updates EEPROM then ADM6996F will update configuration registers.

When CPU programmes EEPROM & ADM6996F, ADM6996F recognizes the EEPROM WRITE instruction only. If there is any Protection instruction before or after the EEPROM WRITE instruction, CPU needs to generate separate CS signal cycles for each Protection & WRITE instruction.

CPU can directly program ADM6996F after 30ms of Reset signal rising edge with or without EEPROM

ADM6996F serial chips will latch hardware-reset value as recommend value. It includes EEPROM interface:

EECS: Internal Pull down 40K resister.

EESK: TP port Auto-MDIX select. Internal pull down 40K resister as non Auto-MDIX mode.

EDI: Dual Color Select. Internal pull down 40K resister as Single Color Mode.

EDO: EEPROM enable. Internal pull up 40K resister as EEPROM enable.

Below Figure is ADM6996F serial chips EEPROM pin operation at different stages. Reset signal is controlled by CPU with at least 100ms low. Point1 is Reset rising edge. CPU must prepare proper values on EECS(0), EESK, EDI, EDO(1) before this rising edge. ADM6996F will read this value into the chip at Point2. CPU must keep these values over point2. Point2 is 200ns after Reset rising edge.

ADM6996F serial chips will read EEPROM content at Point4 which is 800ns away from the rising edge of Reset. CPU must turn EEPROM pins EECS, EESK, EDI and EDO to High-Z or pull high before Point4.

If users want to change the state to High-Z or pull high on EEPROM pins, the order iCS-> DI -> DO -> SK is better.

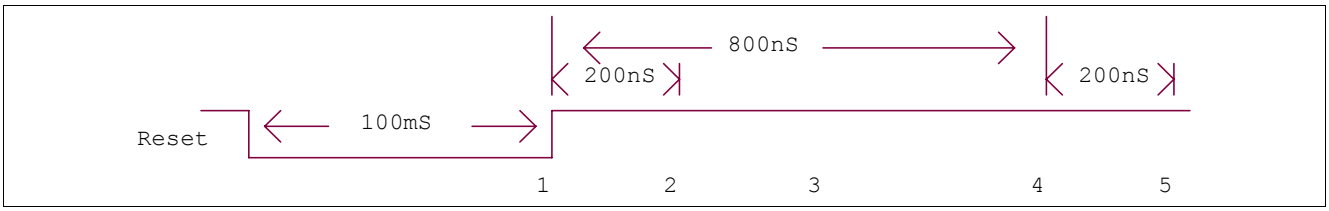


Figure 11 CPU Generated Reset Signal Requirement

The timing for writing to EEPROM is a little different. See the graph below. Must be carefull when CS goes down after writing a command, SK must issue at least one clock. This is a difference between ADM6996F with EEPROM write timing. If the system is without EEPROM then users must write ADM6996F internal register using 93C66 timing. If users use EEPROM then the writing timing depends on EEPROM type.

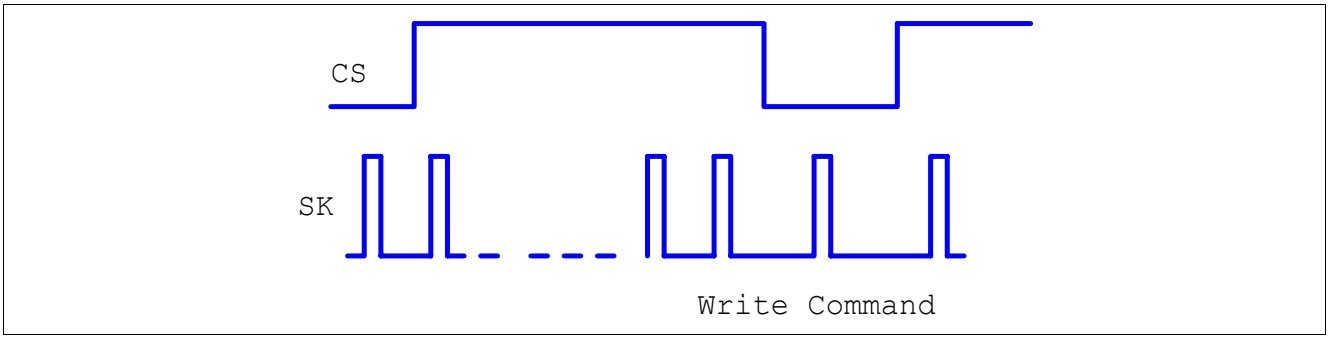


Figure 12 CPU Write EEPROM Command Requirement

4.7 Serial Interface Timing

ADM6996F serial chip's internal counter or EEPROM access timing

EESK: Similar to the MDC signal.

EDI: Similar to the MDIO signal

ECS: Must keep be kept low.

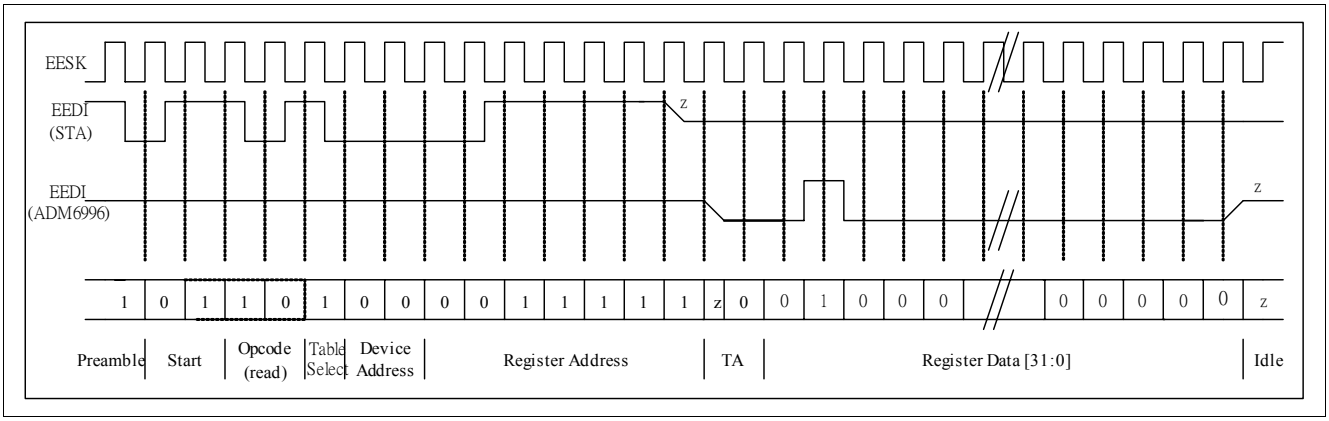


Figure 13 Serial Interface Read Command Timing

Preamble: At least 32 continuous 1_B's

Start: 01_B(2 bits)

Opcode: 10_B (2 bits, Only supports a read command)

Table select: 1_B = Counter, 0_B = EEPROM (1 bit)

Register Address: Read Target register address. (7 bits)

TA: Turn Around.

Register Data: 32 bit data.

Counter output bit sequence is bit 31 to bit 0.

If a user reads the EEPROM then 32 bits of data will be separated in two EEPROM registers. The sequence is:

1. Register +1, Register (Register is even number)
2. Register, Register-1(Register is Odd number)

Example:

Read Register 00_H then the ADM6996F will drive 01_H & 00_H

Read Register 03_H then ADM6996F will drive 03_H & 02_H

Idle: EESK must send at least one clock pulse at idle time

ADM6996F issue Reset internal counter command

EESK: Similar to the MDC signal

EDI: Similar to the MDIO signal

ECS: Must keep low.

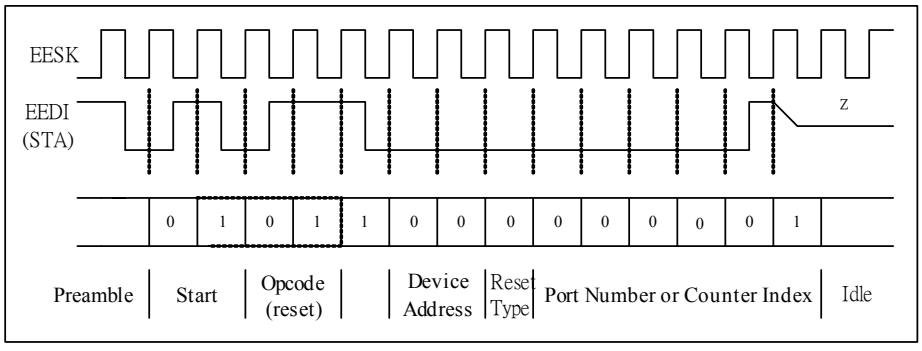


Figure 14 Serial Interface Reset Command Timing

Preamble: At least 32 continuous 1_B's

Start: 01_B(2 bits)

Opcode: 01_B (2 bits, Reset command)

Device Address: Chip physical address as PHYAS[1:0].

Reset_type: Reset the counter by port number or by counter index

1_B = Clear dedicate port's all counters

0_B = Clear dedicate counter

Port_number or counter index: User defines clear port or counter

Idle: EECK must send at least one clock pulse at idle time

4.8 PHY Register Description

Table 30 Registers Address SpaceRegisters Address Space

Module	Base Address	End Address	Note
PHY	00_H	08_H	

Table 31 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
CR	Control Register	00_H	77
SR	Status Register	01_H	79
PHY_IR0	PHY Identifier Register 0	02_H	81
PHY_IR1	PHY Identifier Register 1	03_H	81
ANAR	Auto Negotiation Advertisement Register	04_H	82
ANLPA	Auto Negotiation Link Partner Ability	05_H	83
ANER	Auto Negotiation Expansion Register	06_H	84
NPTR	Next Page Transmit Register	07_H	84
LPNPR	Link Partner Next Page Register	08_H	85

The register is addressed wordwise.

Table 32 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register

Table 32 Register Access Types (cont'd)

Mode	Symbol	Description HW	Description SW
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is read and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW.

Table 33 Registers Clock DomainsRegisters Clock Domains

Clock Short Name	Description

4.8.1 PHY Register Description

Control Register

CR	Offset	Reset Value
Control Register	00_H	3100_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	LPBK	SPD_L	ANEN	PDN	ISO	RSTAR	DPLX	COLTST	SPDMSB	Res					
rwsc	rw	rw	rw	rw	rw	rwsc	rw	rw	ro	ro					

Field	Bits	Type	Description
RST	15	rwsc	**RESET** Setting this bit initiates the software reset function that resets the selected port, except for the phase-lock loop circuit. It will re-latch in all hardware configuration pin values. The software reset process takes 25us to complete. This bit, which is self-clearing, returns a value of 1 when unit the reset process is complete. 0_B **RST_0**, Normal operation 1_B **RST_1**, PHY Reset
LPBK	14	rw	**Loop Back Enable** This bit controls the PHY loop back operation that isolates the network transmitter outputs (TXP and TXN) and routes the MII transmit data to the MII receive data path. This function should only be used when auto negotiation is disabled (bit12 = 0). The specific PHY (10Base-T or 100Base-X) used for this operation is determined by bits 12 and 13. 0_B **LPBK_0**, Disable Loop back mode 1_B **LPBK_1**, Enable loop back mode
SPD_L	13	rw	**Speed Selection LSB** Link speed is selected by this bit or by auto negotiation if bit 12 of this register is set (in which case, the value of this bit is ignored). 00_B **10M**, 10 Mbit/s 01_B **100M**, 100 Mbit/s 10_B **1000M**, 1000 Mbit/s 11_B **Res**, Reserved
ANEN	12	rw	**Auto Negotiation Enable** This bit determines whether the link speed should be set up by the auto negotiation process or not. It is set at power up or reset if the PI_RECANEN pin detects a logic 1 input level in Twisted-Pair Mode.If it is set when fiber mode is configured, any write to this bit will be ignored. 0_B **ANEN_0**, Disable Auto negotiation process 1_B **ANEN_1**, Enable auto negotiation process

Field	Bits	Type	Description
PDN	11	rw	**Power Down Enable** ORed result with PI_PWRDN pin. Setting this bit high or asserting the PI_PWRDN puts the PHY into power down mode. During the power down mode, TXP/TXN and all LED outputs are tri-stated and the MII interfaces are isolated. 0_B **PDN_0**, Normal Operation 1_B **PDN_1**, Power Down
ISO	10	rw	**Isolate PHY from Network** Setting this control bit isolates the part from the RMII/MII, with the exception of the serial management interface. When this bit is asserted, the PHY does not respond to TXD, TXEN and TXER inputs, and it presents a high impedance on its TXC, RXC, CRSDV, RXER, RXD, COL and CRS outputs. 0_B **ISO_0**, Normal Operation 1_B **ISO_1**, Isolate PHY from MII/RMII
RSTAR	9	rwsc	**Restart Auto Negotiation** ANEN_RST. Setting this bit while auto negotiation is enabled forces a new auto negotiation process to start. This bit is self-clearing and returns to 0 after the auto negotiation process has commenced. 0_B **RAN_0**, Normal Operation 1_B **RAN_1**, Restart Auto Negotiation Process
DPLX	8	rw	**Duplex Mode** If auto negotiation is disabled, this bit determines the duplex mode for the link. 0_B **DPLX_0**, Half Duplex mode 1_B **DPLX_1**, Full Duplex mode
COLTST	7	rw	**Collision Test** When set, this bit will cause the COL signal of MII interface to be asserted in response to the assertion of TXEN. 0_B **CT_0**, Disable COL signal test 1_B **CT_1**, Enable COL signal test
SPDMSB	6	ro	**Speed Selection MSB** SPEED_MSB. Set to 0 all the time indicate that the PHY does not support 1000 Mbit/s function.
Res	5:0	ro	**Reserved** Not Applicable.

Status Register

SR	Offset	Reset Value
Status Register	01_H	7849_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPT4	TXFUL	TXHALF	TFUL	THALF	CAPT2	Res			MFSUP	ANCOMP	RMFLT	ANEN	LINK	JAB	EXTCAP
ro	ro	ro	ro	rw	ro	ro			ro	ro	ro	ro	ro	ro	ro

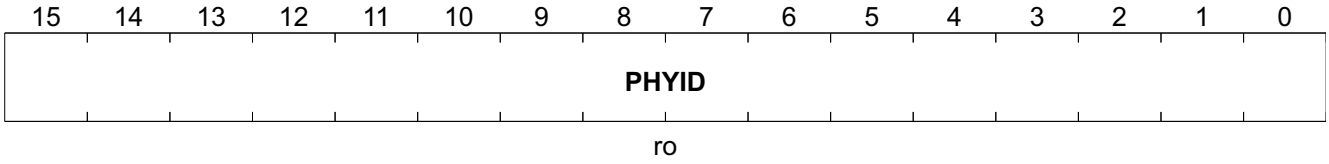
Field	Bits	Type	Description
CAPT4	15	ro	**100Base-T4 Capable** Set to 0 all the time to indicate that the PHY does not support 100Base-T4.
TXFUL	14	ro	**100Base-X Full Duplex Capable** Set to 1 all the time to indicate that the PHY does support Full Duplex mode.
TXHALF	13	ro	**100Base-X Half Duplex Capable** Set to 1 all the time to indicate that the PHY does support Half Duplex mode
TFUL	12	ro	**10M Full Duplex Capable** TP: Set to 1 all the time to indicate that the PHY does support 10M Full Duplex mode. FX: Set to 0 all the time to indicate that the PHY does not support 10M Full Duplex mode
THALF	11	rw	**10M Half Duplex Capable** TP: Set to 1 all the time to indicate that the PHY does support 10M Half Duplex mode. FX: Set to 0 all the time to indicate that the PHY does not support 10M Half Duplex mode
CAPT2	10	ro	**100Base-T2 Capable** Set to 0 all the time to indicate that the PHY does not support 100Base-T2.
Res	9:7	ro	**Reserved** Not Applicable.
MFSUP	6	ro	**MF Preamble Suppression Capable** This bit is hardwired to 1 indicating that the PHY accepts management frame without preamble. Minimum 32 preamble bits are required following power-on or hardware reset. One idle bit is required between any two management transactions as per IEEE 802.3u specification.
ANCOMP	5	ro	**Auto Negotiation Complete** If auto negotiation is enabled, this bit indicates whether the auto negotiation process has been completed or not.Set to 0 all the time when Fiber Mode is selected. 0_B **AN_C_0**, Auto Negotiation process not completed 1_B **AN_C_1**, Auto Negotiation process completed

Field	Bits	Type	Description
RMFLT	4	ro	**Remote Fault Detect** This bit is latched to 1 if the RF bit in the auto negotiation link partner ability register (bit 13, register address 05_H) is set or the receive channel meets the far end fault indication function criteria. It is unlatched when this register is read. 0_B **RFD_0**, Remote Fault not detected. 1_B **RFD_1**, Remote Fault detected
ANEN	3	ro	**Auto Negotiation Ability** TP: This bit is set to 1 all the time, indicating that PHY is capable of auto negotiation. FX: This bit is set to 0 all the time, indicating that PHY is not capable of auto negotiation in Fiber Mode. 0_B **ANEG_0**, Not capable of auto negotiation 1_B **ANEG_1**, Capable of auto negotiation
LINK	2	ro	**Link Status** This bit reflects the current state of the link -test-fail state machine. Loss of a valid link causes a 0 latched into this bit. It remains 0 until this register is read by the serial management interface. Whenever Linkup, this bit should be read twice to get link up status 0_B **LINK_0**, Link is down 1_B **LINK_1**, Link is up
JAB	1	ro	**Jabber Detect** 0_B **JAB_0**, Jabber condition not detected 1_B **JAB_1**, Jabber condition detected
EXTCAP	0	ro	**Extended Capability** This bit defaults to 1, indicating that the PHY implements extended registers. 0_B **XTND_0**, No extended register set 1_B **XTND_1**, Extended register set

PHY Identifier

PHY_IR0 **Offset** **Reset Value**

PHY Identifier Register 0 **02_H** **$002E_H$**

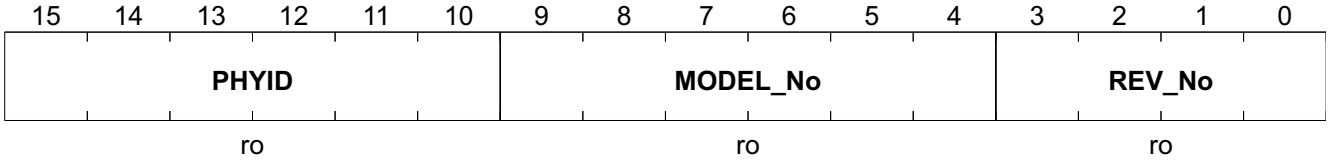


Field	Bits	Type	Description
PHYID	15:0	ro	**IEEE Address**

PHY Identifier Register 1

PHY_IR1 **Offset** **Reset Value**

PHY Identifier Register 1 **03_H** **$CC40_H$**



Field	Bits	Type	Description
PHYID	15:10	ro	**IEEE Address**
MODEL_No	9:4	ro	**IEEE Model No.**
REV_No	3:0	ro	**IEEE Revision No.**

Auto Negotiation Advertisement Register

ANAR	Offset	Reset Value
Auto Negotiation Advertisement Register	04_H	$05E1_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	Res	**RF**	Res	**ASM_DIR**	**PAUSE**	**T4**	**FDX100**	**HDX100**	**FDX10**	**HDX10**	**Selector**				
rw	ro	rw	ro	rw	rw	ro	rw	rw	rw	rw	ro				

Field	Bits	Type	Description
NP	15	rw	**Next Page** This bit is defaults to 1, indicating that PHY is next page capable.
Res	14	ro	**Reserved** Not Applicable
RF	13	rw	**Remote Fault** This bit is written by serial management interface for the purpose of communicating the remote fault condition to the auto negotiation link partner. 0_B **NRFD**, No remote fault has been detected 1_B **RFD**, Remote Fault has been detected
Res	12	ro	**IEEE Reserved** Not Applicable
ASM_DIR	11	rw	**Asymmetric Pause Direction** Bit[11:10] Capability 00_B **NP**, No Pause 01_B **SP**, Symmetric PAUSE 10_B **AP**, Asymmetric PAUSE toward Link Partner 11_B **BSP**, Both Symmetric PAUSE and Asymmetric PAUSE toward local device
PAUSE	10	rw	**Pause Operation for Full Duplex** Value on PAUREC will be stored in this bit during power on reset.
T4	9	ro	**Technology Ability for 100Base-T4** Defaults to 0.
FDX100	8	rw	**100Base-TX Full Duplex** 0_B **NCFDO**, Not capable of 100M Full duplex operation 1_B **CFDO**, Capable of 100M Full duplex operation
HDX100	7	rw	**100Base-TX Half Duplex** 0_B **TXD_0**, Not capable of 100M operation 1_B **TXD_1**, Capable of 100M operation
FDX10	6	rw	**10Base-T Full Duplex** 0_B **TF_0**, Not capable of 10M full duplex operation 1_B **TF_1**, Capable of 10M Full Duplex operation

Field	Bits	Type	Description
HDX10	5	rw	**10Base-T Half Duplex** *Note: bit 8:5 should be combined with REC100, RECFUL pin input to determine the finalized speed and duplex mode.* 0_B **TD_0**, Not capable of 10M operation 1_B **TD_1**, Capable of 10M operation
Selector	4:0	ro	**Selector Field** These 5 bits are hardwired to 00001b, indicating that the PHY supports IEEE 802.3 CSMA/CD.

Auto Negotiation Link Partner Ability

ANLPA	Offset	Reset Value
Auto Negotiation Link Partner Ability	05_H	$01E1_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	**ACK**	**RF**	Res	**LP_DIR**	**LP_PAU**	**LP_T4**	**LP_FDX**	**LP_HDX**	**FDX10**	**HDX10**	**Selector**				
ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro				

Field	Bits	Type	Description
NP	15	ro	**Next Page** 0_B **NPG_0**, Not capable of next page function 1_B **NPG_1**, Capable of next page function
ACK	14	ro	**Acknowledge** 0_B **ACK_0**, Not acknowledged 1_B **ACK_1**, Link Partner acknowledges reception of the ability data word
RF	13	ro	**Remote Fault** 0_B **RF_0**, No remote fault has been detected 1_B **RF_1**, Remote Fault has been detected
Res	12	ro	**Reserved** Not Applicable
LP_DIR	11	ro	**Link Partner Asymmetric Pause Direction**
LP_PAU	10	ro	**Link Partner Pause Capability** Value on PAUREC will be stored in this bit during power on reset.
LP_T4	9	ro	**Link Partner Technology Ability for 100Base-T4** Defaults to 0.
LP_FDX	8	ro	**100Base-TX Full Duplex** 0_B **TXF_0**, Not capable of 100M Full duplex operation 1_B **TXF_1**, Capable of 100M Full duplex operation
LP_HDX	7	ro	**100Base-TX Half Duplex** 1_B **TXD_1**, Capable of 100M operation 0_B **TXD_2**, Not capable of 100M operation

Field	Bits	Type	Description
FDX10	6	ro	**10Base-T Full Duplex** 1_B **TF_1**, Capable of 10M Full Duplex operation 0_B **TF_0**, Not capable of 10M full duplex operation
HDX10	5	ro	**10Base-T Half Duplex** 1_B **TD_1**, Capable of 10M operation 0_B **TD_0**, Not capable of 10M operation
Selector	4:0	ro	**Encoding Definitions**

Auto Negotiation Expansion Register

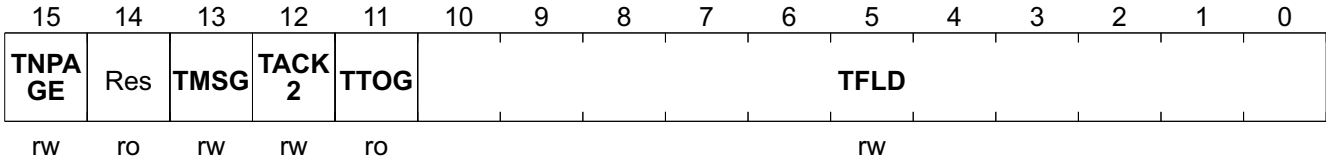
ANER	Offset	Reset Value
Auto Negotiation Expansion Register	**06_H**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res											PDFLT	LPNPAB	NPNBLE	PGRCV	LPANAB
ro											ro, lh	ro	ro	ro, lh	ro

Field	Bits	Type	Description
Res	15:5	ro	**Reserved** Not Applicable
PDFLT	4	ro, lh	**Parallel Detection Fault** 0_B **PFLT_0**, No Fault Detect 1_B **PFLT_1**, Fault has been detected
LPNPAB	3	ro	**Link Partner Next Page Able** 0_B **LPNP_0**, Link Partner is not next page capable 1_B **LPNP_1**, Link Partner is next page capable
NPNBLE	2	ro	**Next Page Able** Defaults to 0, indicating PHY is not capable of next page.
PGRCV	1	ro, lh	**Page Received** 0_B **PRCV_0**, No new page has been received 1_B **PRCV_1**, A new page has been received
LPANAB	0	ro	**Link Partner Auto Negotiation Able** 0_B **LPAN_0**, Link Partner is not auto negotiable 1_B **LPAN_1**, Link Partner is auto negotiable

Next Page Transmit Register

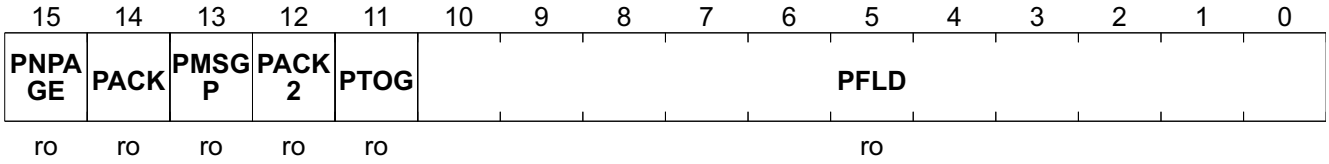
NPTR	Offset	Reset Value
Next Page Transmit Register	**07_H**	**2001_H**



Field	Bits	Type	Description
TNPAGE	15	rw	**Transmit Next Page** Transmit Code Word Bit15
Res	14	ro	**Reserved** Not Applicable
TMSG	13	rw	**Transmit Message Page** Transmit Code Word Bit13
TACK2	12	rw	**Transmit Acknowledge 2** Transmit Code Word Bit12
TTOG	11	ro	**Transmit Toggle** Transmit Code Word Bit11
TFLD	10:0	rw	**Transmit Message Field** Transmit Code Word Bit10...0

Link Partner Next Page Register

LPNPR	Offset	Reset Value
Link Partner Next Page Register	**08_H**	**0000_H**



Field	Bits	Type	Description
PNPAGE	15	ro	**Link Partner Next Page** Receive Code Word Bit15
PACK	14	ro	**Link Partner Acknowledge** Receive Code Word Bit14
PMSGP	13	ro	**Link Partner Message Page** Receive Code Word Bit13
PACK2	12	ro	**Link Partner Acknowledge 2** Receive Code Word Bit12
PTOG	11	ro	**Link Partner Toggle** Receive Code Word Bit11
PFLD	10:0	ro	**Link Partner Message Field** Receive Code Word Bit10...0

4.9 Management Interface for PHY Register Access

The SMI consists of two pins, management data clock (MDC) and management data input/output (MDIO). The ADM6996F is designed to support an MDC frequency specified in the IEEE specification of up to 2.5 MHz. The MDIO line is bi-directional and may be shared by up to 32 devices.

The MDIO pin requires a 1.5 kOhm pull-up which, during idle and turnaround periods, will pull MDIO to a logic one state. Each PHY register data frame is 64 bits long. The first 32 bits are preamble consisting of 32 contiguous logic one bits on MDIO and 32 corresponding cycles on MDC. Following preamble is the start-of-frame field indicated by a <01> pattern. The next field signals the operation code (OP) : <10> indicates read from PHY register operation, and <01> indicates write to PHY register operation. The next two fields are PHY device address and PHY register address. Both of them are 5 bits wide and the most significant bit is transferred first.

During Read operation, a 2-bit turn around (TA) time spacing between the register address field and data field is provided for the MDIO to avoid contention. Following the turnaround time, a 16-bit data stream is read from or written into the PHY registers of the ADM6996F.

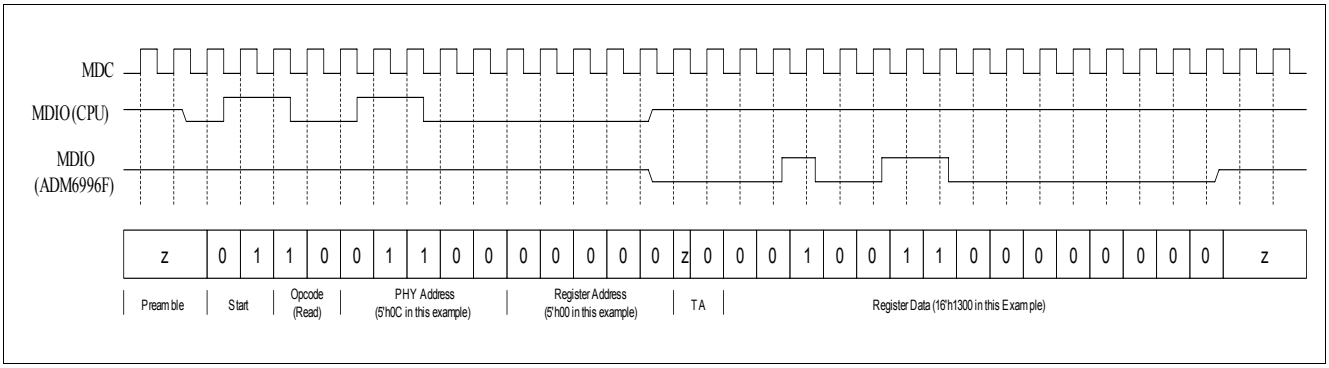


Figure 15 SMI Read Operation

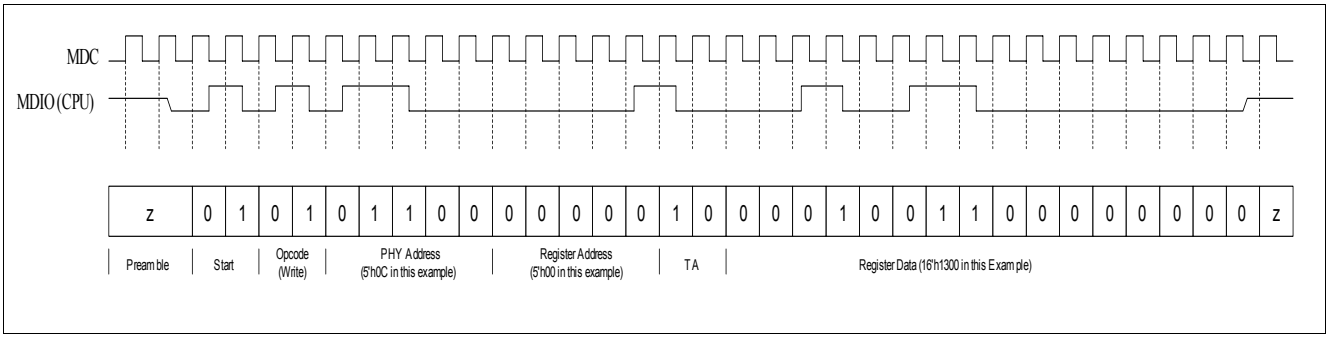


Figure 16 SMI Write Operation

5 Electrical Specification

5.1 TX/FX Interface

5.1.1 TP Interface

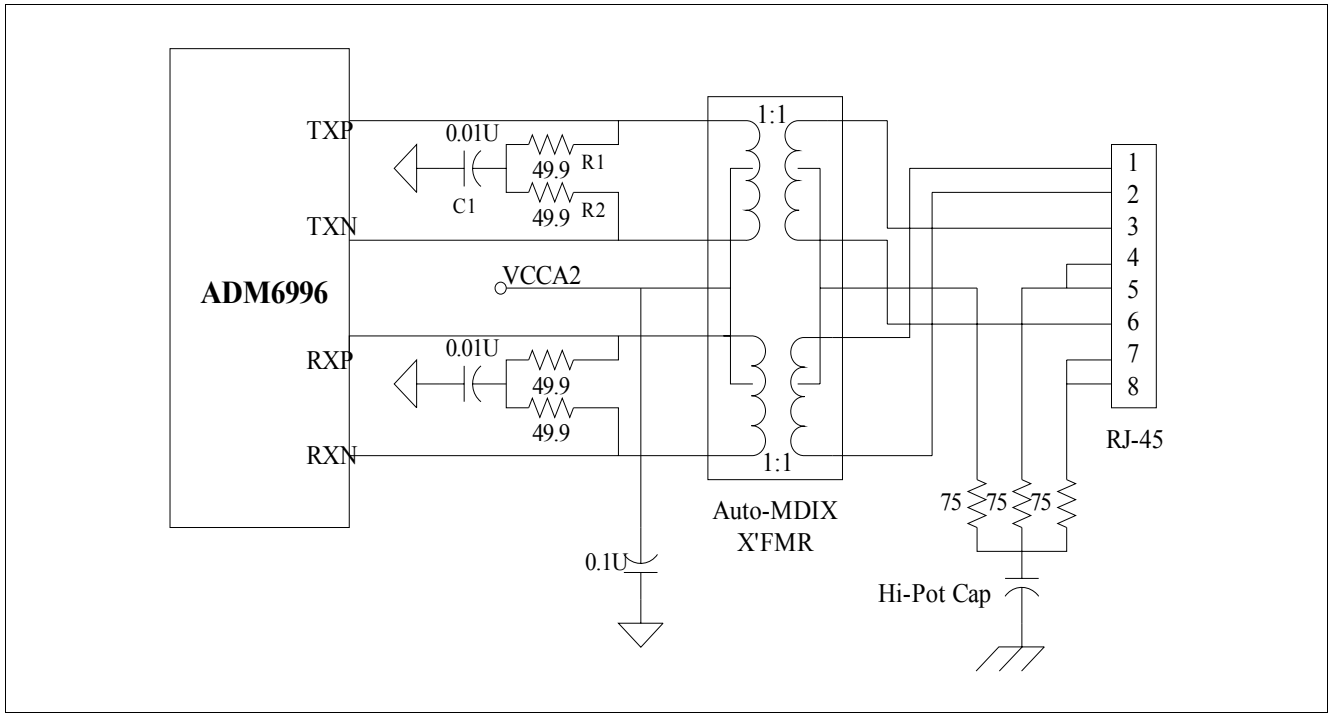


Figure 17 TP Interface

Transformer requirements:

- TX/RX rate 1:1
- TX/RX central tap connect together to VCCA2

Users can change the TX/RX pin for ease of layout but do not change the polarity. Samurai-6FC (ADM6996FC) supports auto polarity on the receiving side.

5.1.2 FX Interface

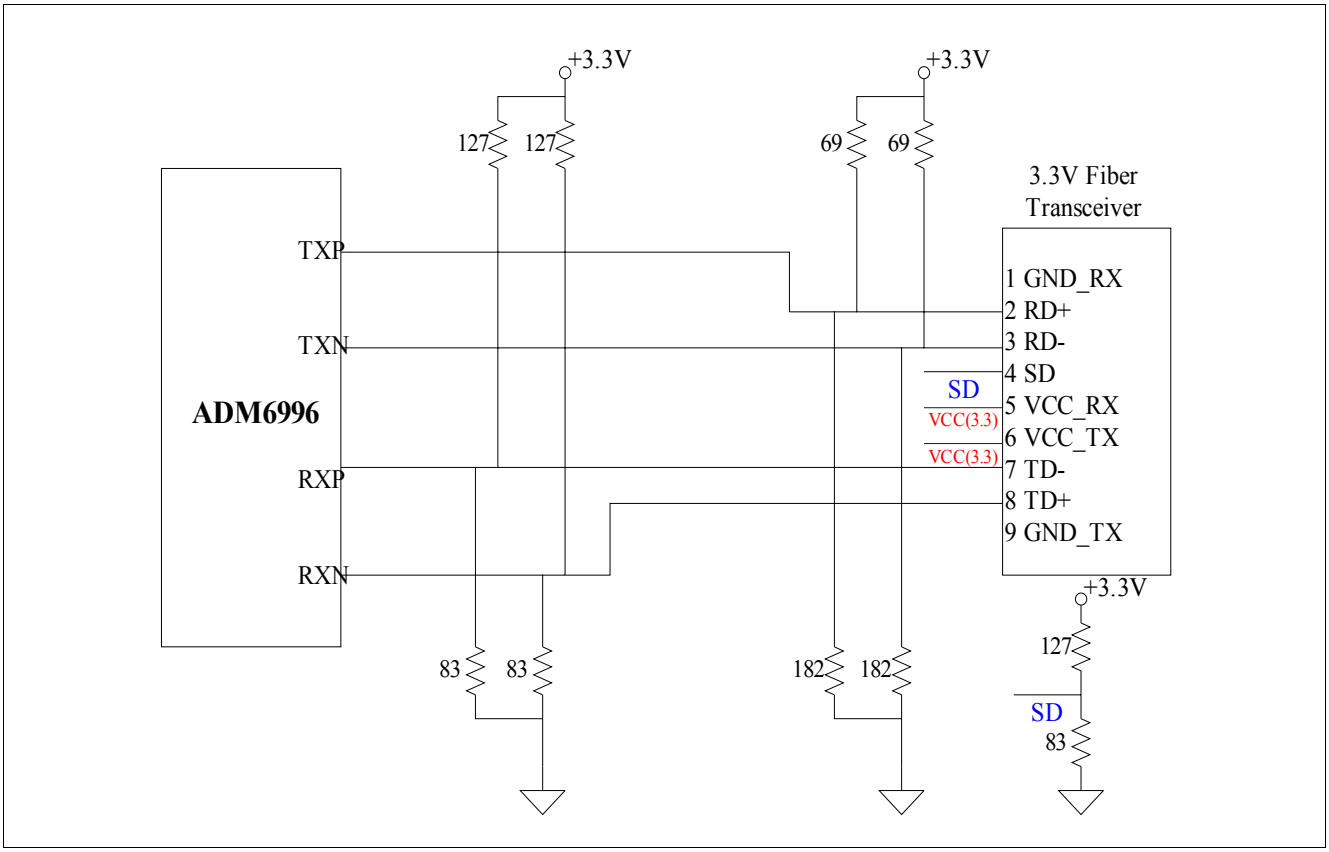


Figure 18 FX Interface

5.2 DC Characteristics

5.2.1 Absolute Maximum Rating

Table 34 Absolute Maximum Rating

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply	V_{CC}	-0.3		3.63	V	
TX line driver	*Vcca2*			1.8	V	
PLL voltage	*Vccpll*			1.8	V	
Digital core voltage	*Vccik*			1.8	V	
Input Voltage	V_{IN}	-0.3		V CC + 0.3	V	
Output Voltage	*Vout*	-0.3		Vcc + 0.3	V	
Storage Temperature	*TSTG*	-55		155	C	

Table 34 Absolute Maximum Rating (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Dissipation	*PD*			1.3W	W	
ESD Rating	*ESD*			2KV	V	

5.2.2 Recommended Operating Conditions

Table 35 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply	*Vcc*	2.8	3.3	3.465	V	
TX line driver	*Vcca2*	1.7	1.8	1.9	V	
PLL voltage	*Vccpll*	1.7	1.8	1.9	V	
Digital core voltage	*Vccik*	1.7	1.8	1.9	V	
Input Voltage	*Vin*	0	-	Vcc	V	
Power consumption	*PC*		1.3		W	
Junction Operating Temperature	*Tj*	0	25	115	C	

5.2.3 DC Electrical Characteristics for 3.3 V Operation

Under Vcc=3.0 V~3.6 V, Tj= 0 C ~ 115 C

Table 36 DC Electrical Characteristics for 3.3 V Operation

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Low Voltage	*VIL*			0.3 * Vcc	V	CMOS
Input High Voltage	*VIH*	0.7 * Vcc			V	CMOS
Output Low Voltage	*VOL*			0.4	V	CMOS
Output High Voltage	*VOH*	0.7 * Vcc			V	CMOS
Input Pull_up/down Resistance	*RI*		100		K	VIL=0 V or VIH = Vcc

Note: 100BaseT Full Duplex: 130mA (3.3 V) 500mA (1.8 V) => 1.329W

Note: 10BaseT Full Duplex: 50mA (3.3 V) 740mA (1.8 V) => 1.497W

Note: No Link: 30mA (3.3 V) 580mA (1.8 V) => 1.143W

5.3 AC Characterization

5.3.1 XTAL/OSC Timing

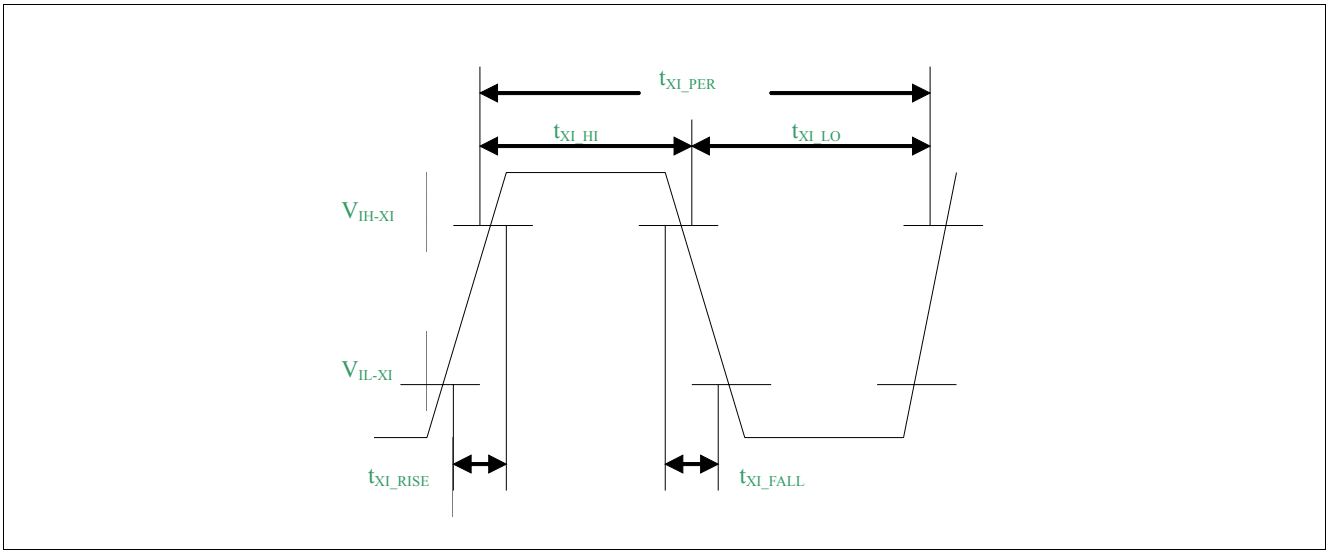


Figure 19 XTAL/OSC Timing

Table 37 XTAL/OSC Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
XI/OSCI Clock Period	$t_{\_XI\_PER}$	40.0 - 50ppm	40.0	40.0 + 50ppm	ns	–
XI/OSCI Clock High	$t_{\_XI\_HI}$	14	20.0	–	ns	–
XI/OSCI Clock Low	$t_{\_XI\_LO}$	14	20.0	–	ns	–
XI/OSCI Clock Rise Time, V_{IL} (max) to V_{IH} (min.)	$t_{\_XI\_RISE}$	–	–	4	ns	–
XI/OSCI Clock Fall Time, V_{IH} (min.) to V_{IL} (max)	$t_{\_XI\_FALL}$	–	–	4	ns	–

5.3.2 Power On Reset

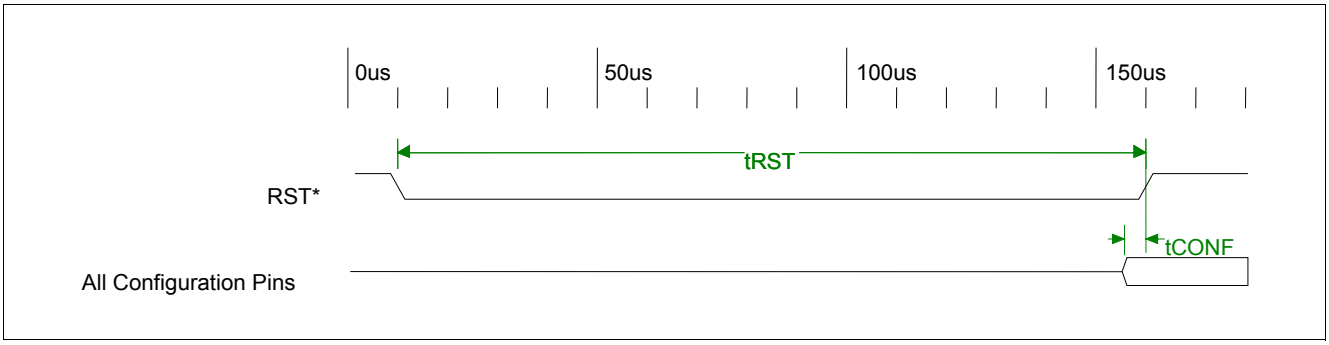


Figure 20 Power On Reset Timing

Table 38 Power On Reset Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RST Low Period	t_{RST}	100	–	–	ms	–
Start of Idle Pulse Width	t_{CONF}	100	–	–	ns	–

5.3.3 EEPROM Interface Timing

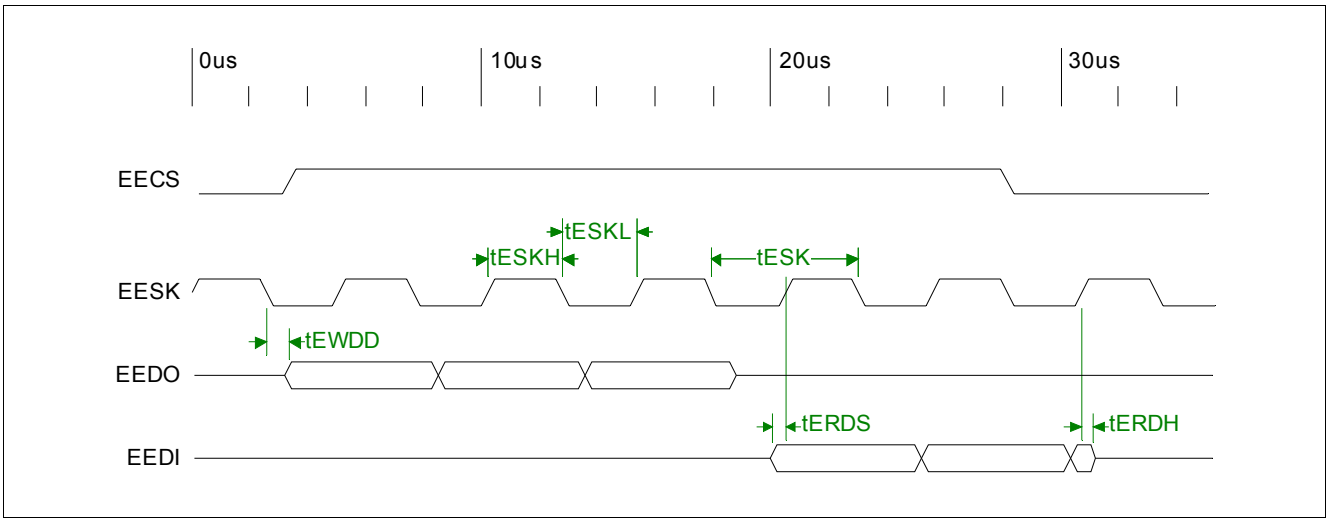


Figure 21 EEPROM Interface Timing

Table 39 EEPROM Interface Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EESK Period	t_{ESK}	–	5120	–	ns	–
EESK Low Period	t_{ESKL}	2550	–	2570	ns	–
EESK High Period	t_{ESKH}	2550	–	2570	ns	–
EEDI to EESK Rising Setup Time	t_{ERDS}	10	–	–	ns	–
EEDI to EESK Rising Hold Time	t_{ERDH}	10	–	–	ns	–
EESK Falling to EEDO Output Delay Time	t_{EWDD}	–	–	20	ns	–

5.3.4 10Base-TX MII Input Timing

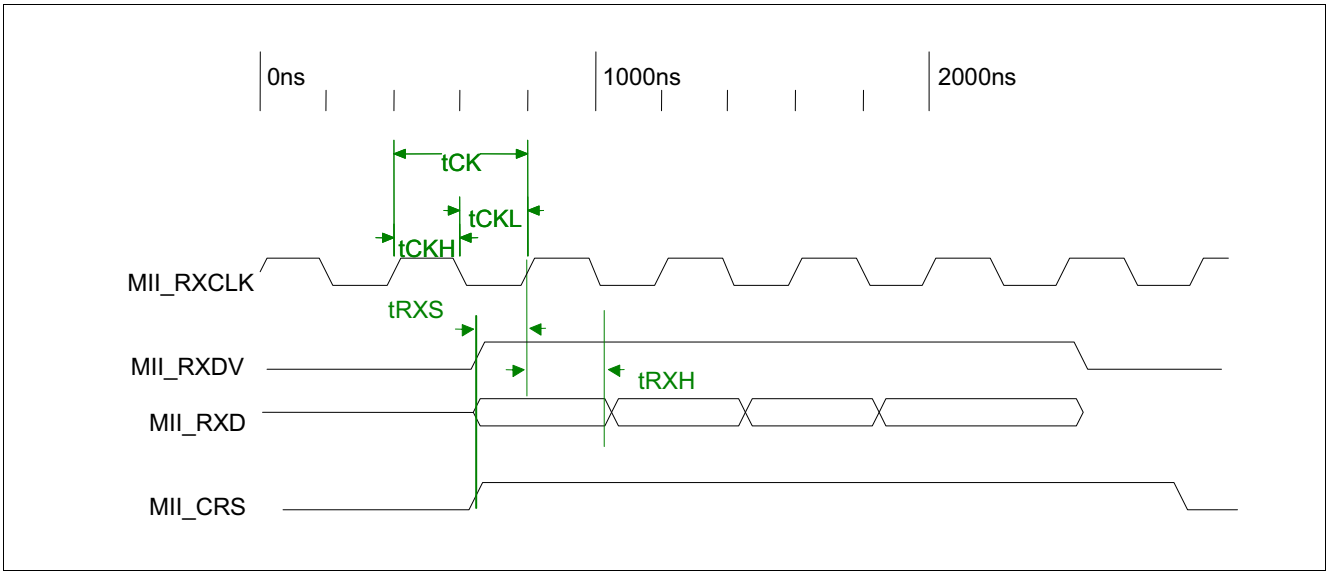


Figure 22 10Base-TX MII Input Timing

Table 40 10Base-TX MII Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_RXCLK Period	t_{CK}	–	400	–	ns	–
MII_RXCLK Low Period	t_{CKL}	180	–	220	ns	–
MII_RXCLK High Period	t_{CKH}	180	–	220	ns	–
MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising setup	t_{RXS}	10	–	–	ns	–
MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising hold	t_{RXH}	10	–	–	ns	–

5.3.5 10Base-TX MII Output Timing

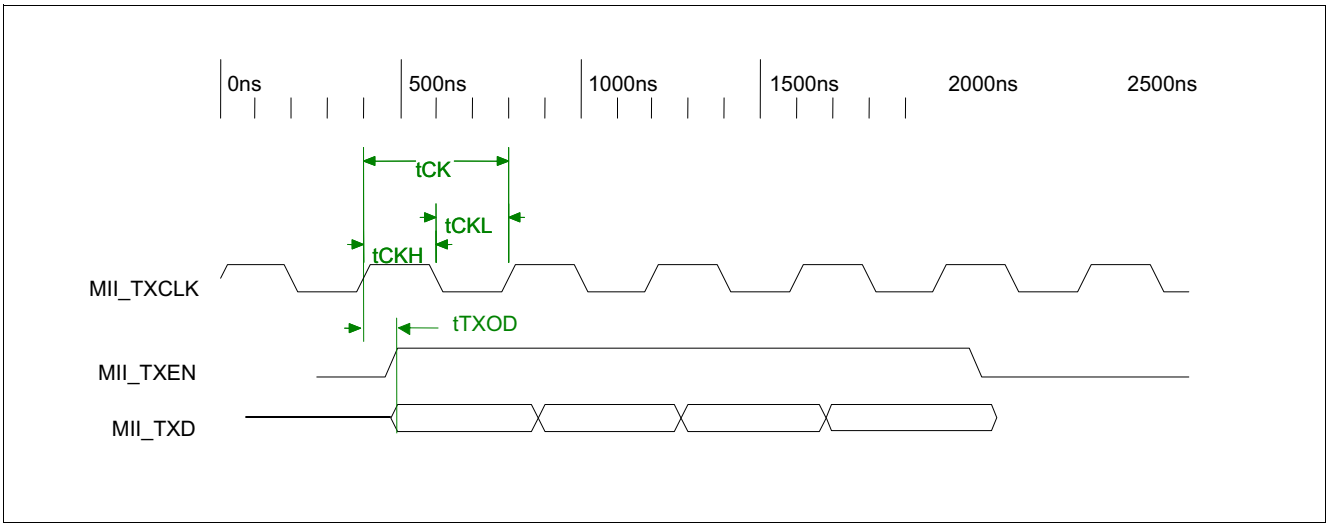


Figure 23 10Base-TX MII Output Timing

Table 41 10-Base-TX MII Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_TXCLK Period	t_{CK}	–	400	–	ns	–
MII_TXCLK Low Period	t_{CKL}	180	–	220	ns	–
MII_TXCLK High Period	t_{CKH}	180	–	220	ns	–
MII_TXD, MII_TXEN to MII_TXCLK Rising Output Delay	t_{TXOD}	0	–	25	ns	–

5.3.6 100Base-TX MII Input Timing

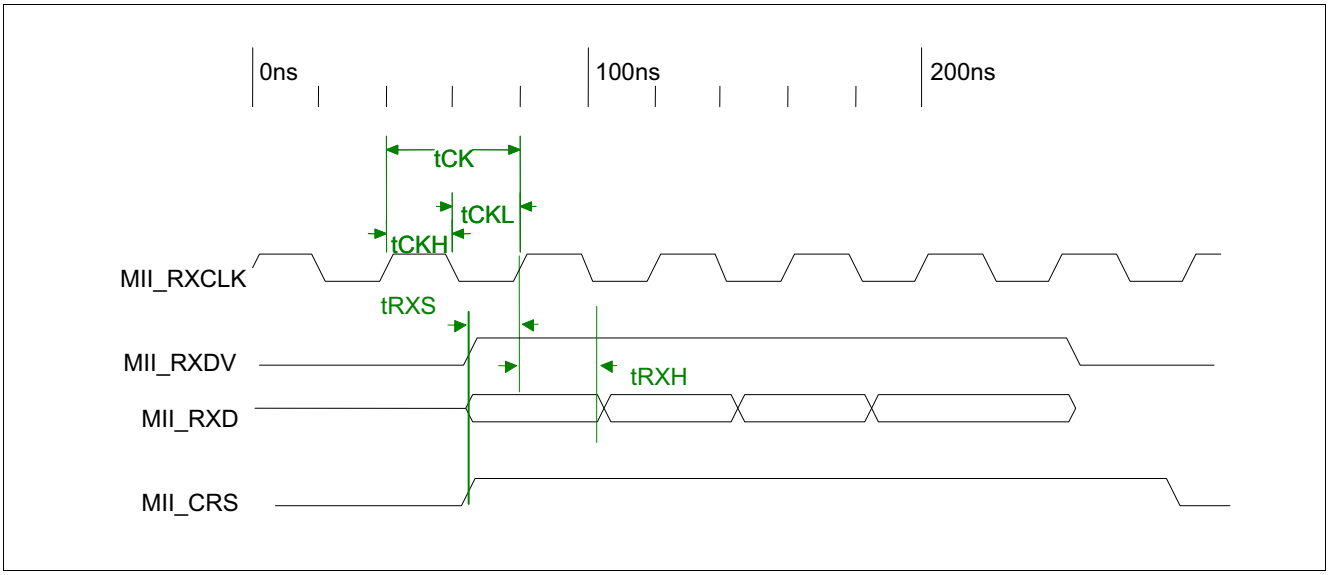


Figure 24 100Base-TX MII Input Timing

Table 42 100Base-TX MII Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_RXCLK Period	t_{CK}	–	40	–	ns	–
MII_RXCLK Low Period	t_{CKL}	18	–	22	ns	–
MII_RXCLK High Period	t_{CKH}	18	–	22	ns	–
MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising setup	t_{RXS}	10	–	–	ns	–
MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising hold	t_{RXH}	10	–	–	ns	–

5.3.7 100Base-TX MII Output Timing

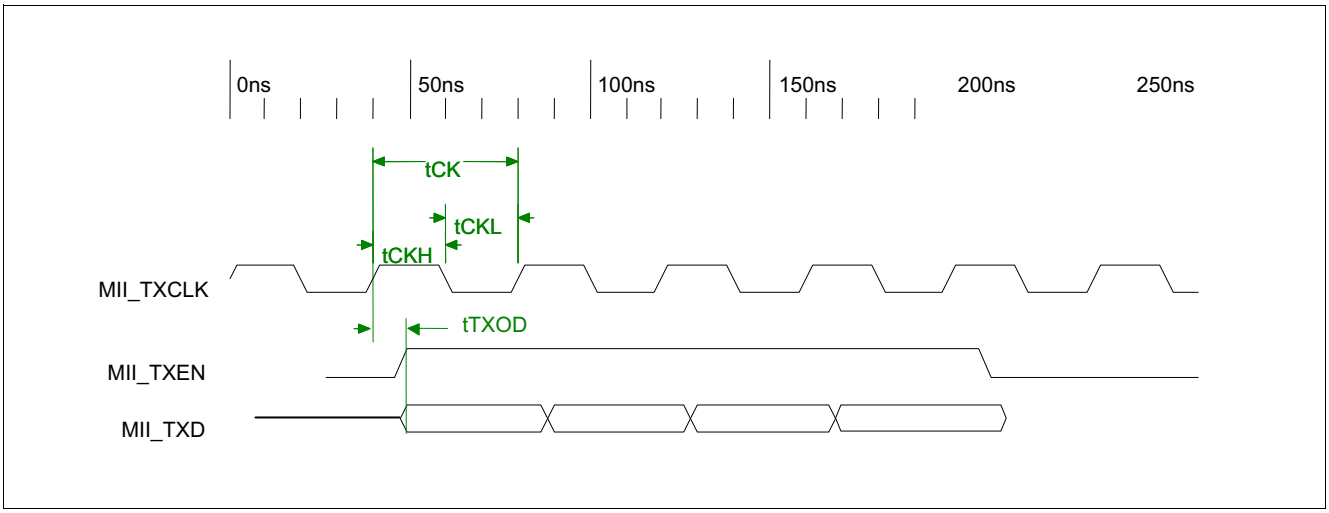


Figure 25 100Base-TX MII Output Timing

Table 43 100Base-TX MII Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_TXCLK Period	t_{CK}	–	40	–	ns	–
MII_TXCLK Low Period	t_{CKL}	18	–	22	ns	–
MII_TXCLK High Period	t_{CKH}	18	–	22	ns	–
MII_TXD, MII_TXEN to MII_TXCLK Rising Output Delay	t_{TXOD}	0	–	25	ns	–

5.3.8 GPSI (7-wire) Input Timing

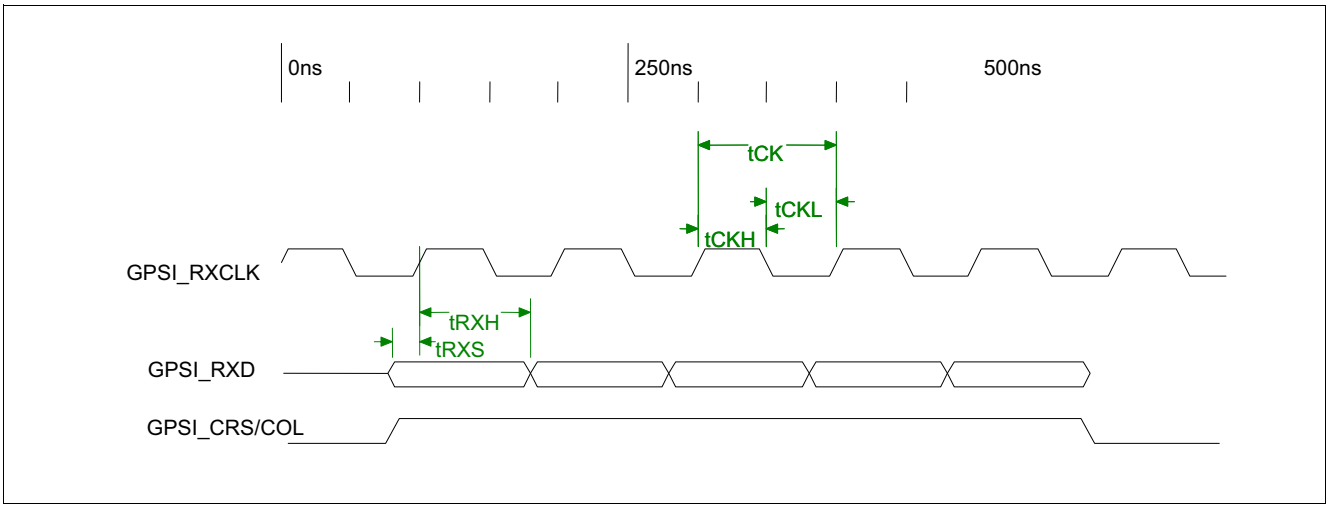


Figure 26 GPSI (7-wire) Input Timing

Table 44 GPSI (7-wire) Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
GPSI_RXCLK Period	t_{CK}	–	100	–	ns	–
GPSI_RXCLK Low Period	t_{CKL}	40	–	60	ns	–
GPSI_RXCLK High Period	t_{CKH}	40	–	60	ns	–
GPSI_RXD, GPSI_CRS/COL to GPSI_RXCLK Rising Setup Time	t_{RXS}	10	–	–	ns	–
GPSI_RXD, GPSI_CRS/COL to GPSI_RXCLK Rising HoldTime	t_{RXH}	10	–	–	ns	–

5.3.9 GPSI (7-wire) Output Timing

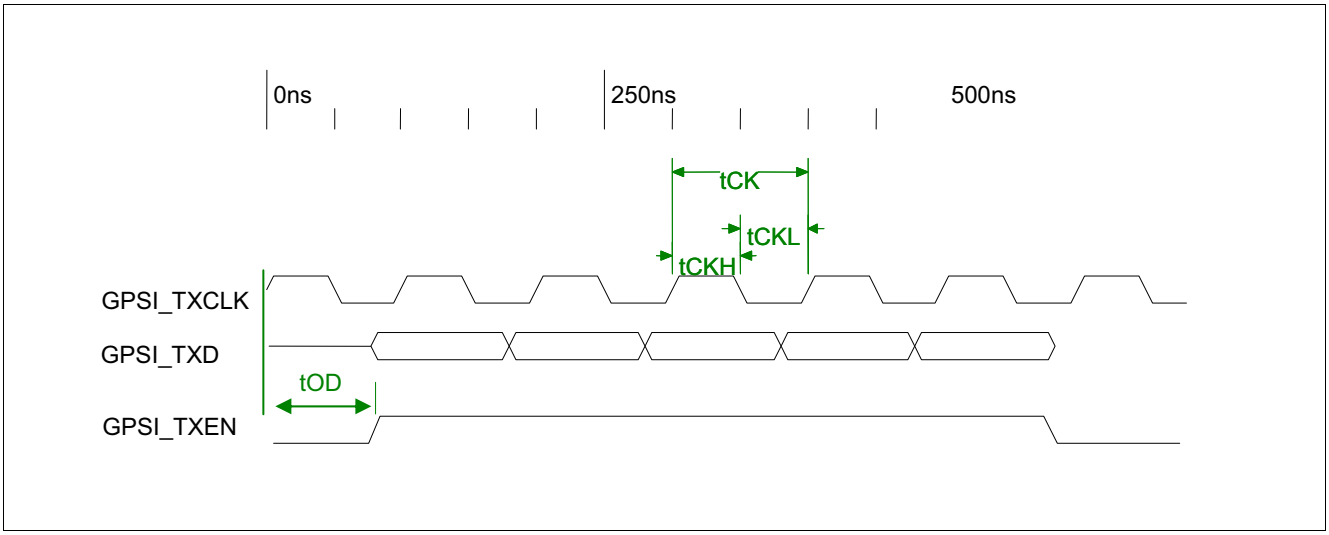


Figure 27 GPSI (7-wire) Output Timing

Table 45 GPSI (7-wire) Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
GPSI_TXCLK Period	t_{CK}	–	100	–	ns	–
GPSI_TXCLK Low Period	t_{CKL}	40	–	60	ns	–
GPSI_TXCLK High Period	t_{CKH}	40	–	60	ns	–
GPSI_TXCLK Rising to GPSI_TXEN/GPSI_TXD Output Delay	t_{OD}	50	–	70	ns	–

5.3.10 SDC/SDIO Timing

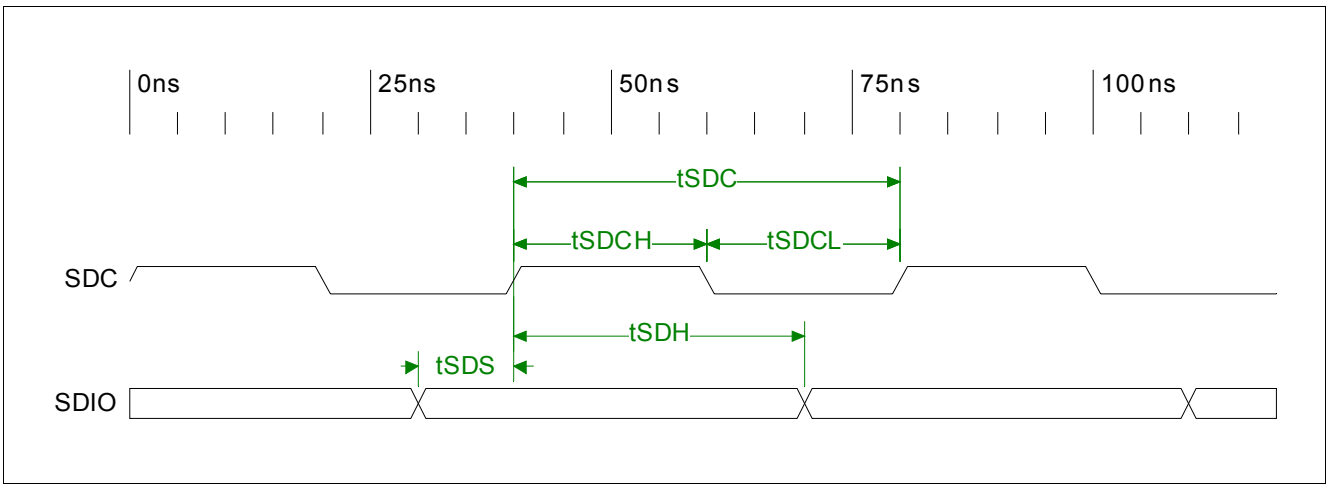


Figure 28 SDC/SDIO Timing

Table 46 SDC/SDIO Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SDC Period	t_{CK}	20	–	–	ns	–
SDC Low Period	t_{CKL}	10	–	–	ns	–
SDC High Period	t_{CKH}	10	–	–	ns	–
SDIO to SDC rising setup time on read/write cycle	t_{SDS}	4	–	–	ns	–
SDIO to SDC rising hold time on read/write cycle	t_{SDH}	2	–	–	ns	–

5.3.11 MDC/MDIO Timing

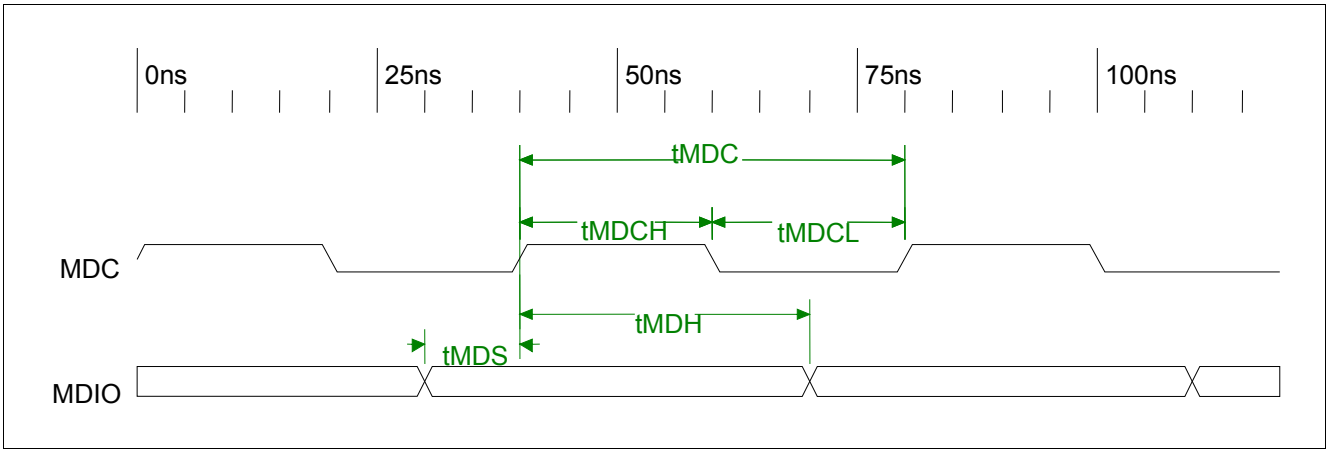
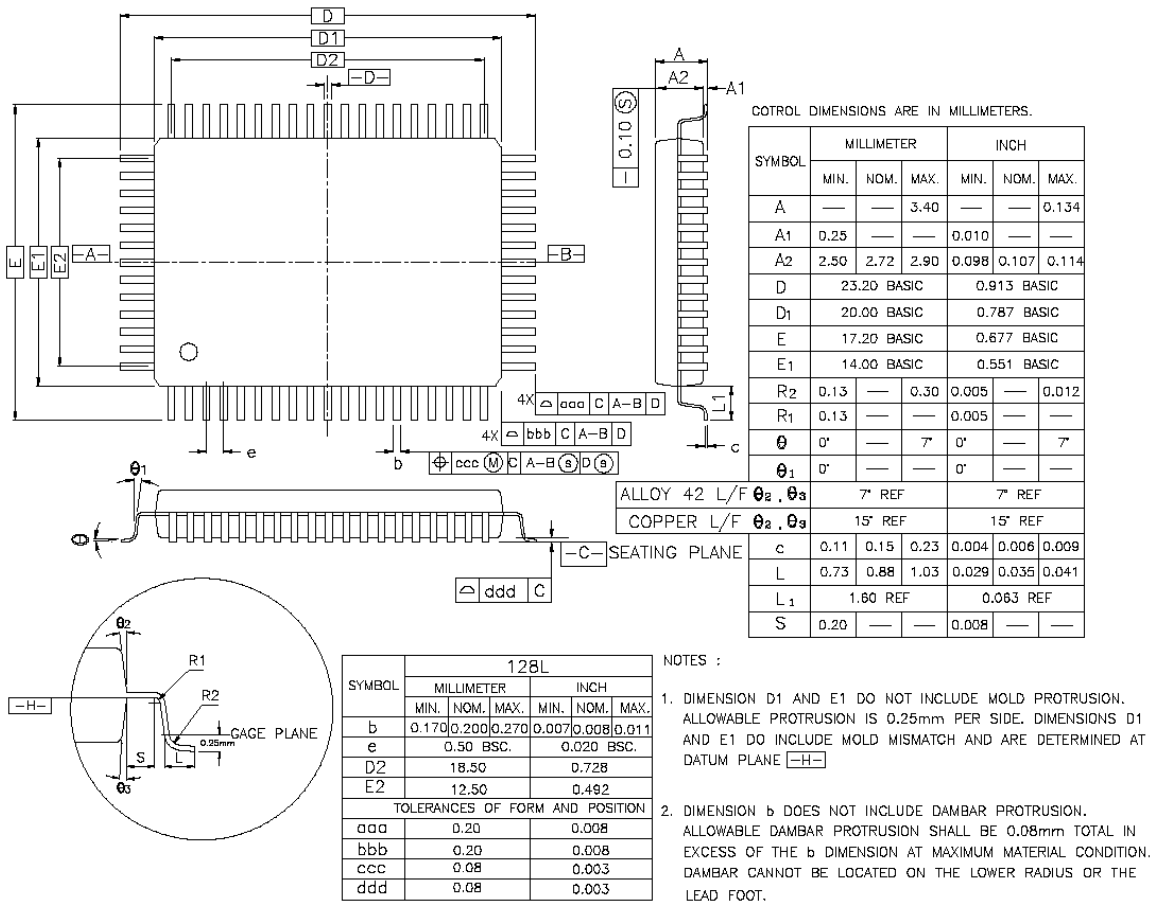


Figure 29 MDC/MDIO Timing

Table 47 MDC/MDIO Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MDC Period	t_{MDC}	100	–	–	ns	–
MDC Low Period	t_{MDCL}	40	–	–	ns	–
MDC High Period	t_{MDCH}	40	–	–	ns	–
MDIO to MDC rising setup time on read/write cycle	t_{MDS}	–	–	10	ns	–
MDIO to MDC rising hold time on read/write cycle	t_{MDH}	10	–	–	ns	–

6 Package Outlines



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
ALLOY 42 L/F θ2, θ3	7° REF			7° REF		
COPPER L/F θ2, θ3	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	128L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.170	0.200	0.270	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

Figure 30 P-PQFP-128 Outside Dimension

6.1 Package Information

Product Name	Product Type	Package
6-Port 10/100 Mbit/s Single Chip Ethernet Switch Controller	ADM6996F, ADM6996F-AA-T-1, Version AA	P-PQFP-128

Terminology

B	
BER	Bit Error Rate
C	
CFI	Canonical Format Indicator
COL	Collision
CRC	Cyclic Redundancy Check
CRS	Carrier Sense
CS	Chip Select
D	
DA	Destination Address
DI	Data Input
DO	Data Output
E	
EDI	EEPROM Data Input
EDO	EEPROM Data Output
EECS	EEPROM Chip Select
EESK	EEPROM Clock
ESD	End of Stream Delimiter
F	
FEFI	Far End Fault Indication
FET	Field Effect Transistor
FLP	Fast Link Pulse
G	
GND	Ground
GPSI	General Purpose Serial Interface
I	
IPG	Inter-Packet Gap
L	
LFSR	Linear Feedback Shift Register
M	
MAC	Media Access Controller
MDIX	MDI Crossover
MII	Media Independent Interface
N	
NRZI	Non Return to Zero Inverter
NRZ	Non Return to Zero
P	
PCS	Physical Coding Sub-layer
PHY	Physical Layer
PLL	Phase Lock Loop
PMA	Physical Medium Attachment

PMD	Physical Medium Dependent
Q	
QoS	Quality of Service
QFP	Quad Flat Package
R	
RST	Reset
RXCLK	Receive Clock
RXD	Receive Data
RXDV	Receive Data Valid
RXER	Receive Data Errors
RXN	Receive Negative (Analog receive differential signal)
RXP	Receive Positive (Analog receive differential signal)
S	
SA	Source Address
SOHO	Small Office Home Office
SSD	Start of Stream Delimiter
SQE	Signal Quality Error
T	
TOS	Type of Service
TP	Twisted Pair
TTL	Transistor Logic
TXCLK	Transmission Clock
TXD	Transmission Data
TXEN	Transmission Enable
TXN	Transmission Negative
TXP	Transmission Positive

www.infineon.com

Published by Infineon Technologies AG